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A study of the effect of temperature changes on the interpolating time counter

Abstract

This paper presents an analysis of the impact of ambient temperature changes on main parameters of the interpolating time counter. The performed tests reveal that a relatively small change in the ambient temperature of 1°C causes a measurement error of the counter as large as 3.5 ps. The thorough research of two stages of interpolation of the counter allowed determining the main sources of the error. One of them is the temperature drift of widths of four-phase clock (FPC) segments in the first interpolation stage (FIS). It equals 2.5 ps/°C. The widths of FPC phases directly influence the active range of the second interpolation stage (SIS) and its offset. The test results also show that the temperature drift of the offset has a greater impact on the measurement accuracy than the temperature-driven changes of quantization steps in SIS. The presented conclusions are the first step to develop a new method for reducing the impact of changes in the ambient temperature on the measurement accuracy of the interpolating time counter.

Keywords: time interval measurement, time-to-digital conversion, two-stage interpolation, time counter, temperature effect.

1. Introduction

The direct time-to-digital conversion method based on the use of a single discrete coding line is the most popular digital method implemented in integrated circuits (ICs) for precise time interval measurements [1, 2]. A typical discrete coding line is implemented as a chain of delay buffers and related D flip-flops. In FPGA devices, the fast carry chain structure is usually used for that purpose. Since the propagation time of delay elements of the built-in carry chain is very sensitive to power supply voltage and temperature drift, their variations can significantly deteriorate the measurement precision [3]. The supply voltage variations can be effectively minimized by using a low noise and low dropout regulator. However, the elimination of temperature variations is more difficult. Most often integrated time counters (TCs) are placed in sealed enclosures in order to minimize these changes. Moreover, before each measurement session TCs are subjected to a warm-up process. Unfortunately, such an additional non-measurement step is time consuming and should be omitted. One way of dealing with this problem is to repeat the calibration procedure, in which the quantization steps of a delay line are carefully identified. The converter calibration procedure is performed obligatory once during the start of the converter and next after each significant change in the temperature. Since the calibrations should not interrupt a measurement session, this solution cannot be applied during long sessions. Another solution, proposed in this paper, is the measurement result correction based on the use of a certain coefficient, whose value depends on the scale of a change in the ambient temperature. However, in order to apply this method, precise identification of the TC errors due to changes in the ambient temperature is required. This paper presents the test results of the temperature influence on the measurement parameters of the interpolation TC implemented in an FPGA device. The main attention is focused on the errors occurring in time interpolators. The effect of temperature on the parameters of the input circuits and the jitter of clock signals supplied to the TC are omitted.

2. The interpolating time counter with multi-edge coding in independent coding lines

For precise measurement of long time intervals the two-stage interpolation method (Fig. 1a), being an advanced version of the classical Nutt method [1], is commonly used. In this method, the time interval T_M is measured first by an ordinary binary counter that counts an integer number of the reference clock periods, which appear between the leading edges of START and STOP pulses. Time intervals between the active edges of pulses and the nearest edges of the reference clock are measured by two-stage interpolators. The first interpolation stage (FIS) determines the phases of a multiphase clock in which the edges of input pulses appear. Subsequently, the intervals T_{ST1} and T_{SP1} are calculated based on the known durations of the multiphase clock phases. The second interpolation stage (SIS) measures the times T_{SP2} and T_{ST2} between the START and STOP edges, and the nearest edges of the multiphase clock, respectively. The TC was implemented in a Spartan-6 (*Xilinx*) device. In the FIS of both interpolators a four-phase clock (FPC) was applied. The simplified block diagram of the designed TC is shown in Fig. 1b, while the detailed description of the conversion method and its implementation is presented in [4, 5].

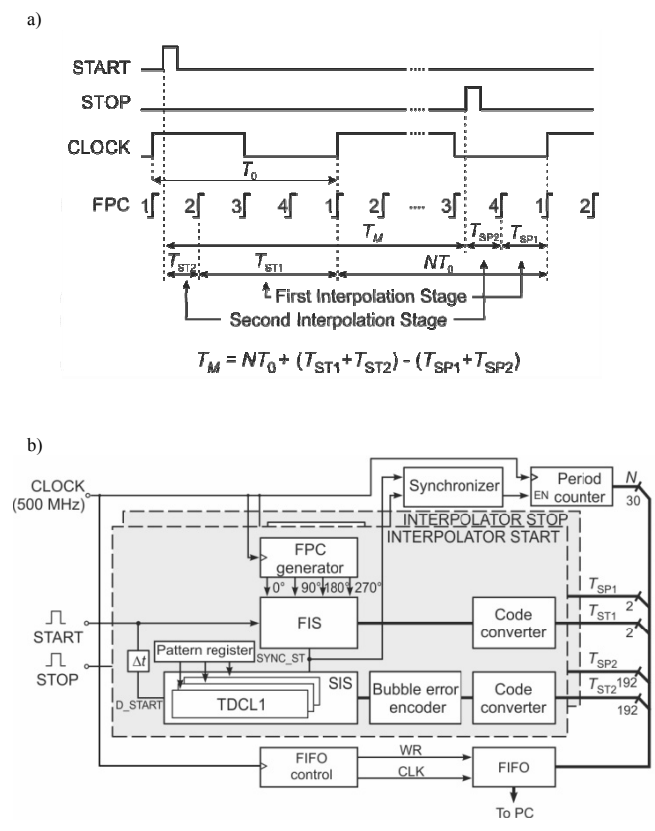

Fig. 1. a) Two-stage interpolation method, b) simplified block diagram of the interpolating time counter

The experimental tests of the designed TC were evaluated with the use of a dedicated test board, which contained the Spartan-6 (*Xilinx*) device, DDR memory for fast storing the measurement data, and a synthesizer that generated a 500 MHz reference clock.

3. Impact of the ambient temperature on the FIS

Generally, to create an FPC in the FIS, either a generator based on a differential delay line [3] or a tapped delay line [6] is used. In

the presented case, the second type of a generator was applied. Its structure, which consists of two buffers and two inverters, is shown in Fig. 2a. Both buffers and inverters were implemented in look-up tables.

In the first test, we verified the influence of temperature on the FIS in the interpolators START and STOP. The temperature tests were performed with the aid of a thermal chamber PL-2J (*ESPEC*). In order to identify the phase widths of FPC, a statistical code density test [7] was conducted in several different ambient temperatures (−10°C, 10°C, 25°C, 40°C, 60°C). The obtained phase widths for both interpolators are very similar, therefore they are presented only for the START interpolator (Fig. 2b). The widths and their changes with the drift of temperature are strictly related to the propagation time of elements used to build the FPC generator. The temperature drift of 1°C causes a 2.5 ps change in the widths of the phase segments of FPC.

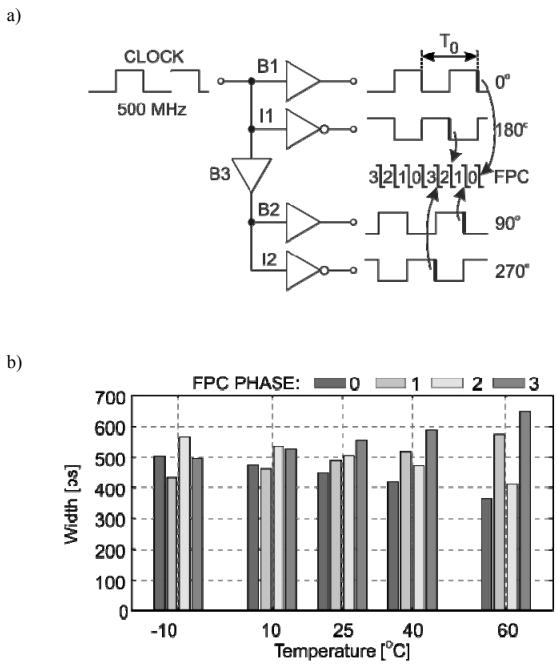

Fig. 2. a) Schematic diagram of the FPC generation method, b) widths of FPC phases in the START channel obtained in different ambient temperatures

In the ideal case, in which the buffer delay of B3 would be equal to ¼ T_0 and the delays of other buffers and inverters would be the same, the width of each phase would amount exactly to ¼ T_0. It is difficult to obtain the assumed delays under real conditions and actual widths of phases differ one from another. In addition, as it is shown in Fig. 2b, the widths of phases 0 and 2 are slightly reduced, whereas the phases 1 and 3 are expanded with the increasing temperature. This effect is related to the change in the propagation time of buffer B3. Changes in the propagation time of other buffers and inverters do not affect significantly the widths of phases.

4. Impact of the ambient temperature on the SIS

In the SIS of each interpolator, a precise time-to-digital converter (TDC) based on the method of multi-edge coding in independent coding lines (MECICL) was used [3]. The TDC consists of three discrete delay lines through which a six-edge pattern is propagated. Such a structure of the TDC allows achieving the high resolution of conversion, below 1 ps, and the low occupancy of logical resources of the FPGA device. As in the previous study, in order to identify the influence of temperature on the SIS, we performed the research in which the TDC transfer functions were identified in several temperatures enumerated previously. The widths of the TDC quantization steps for the phase 0 of the FPC are shown in Fig. 3a.

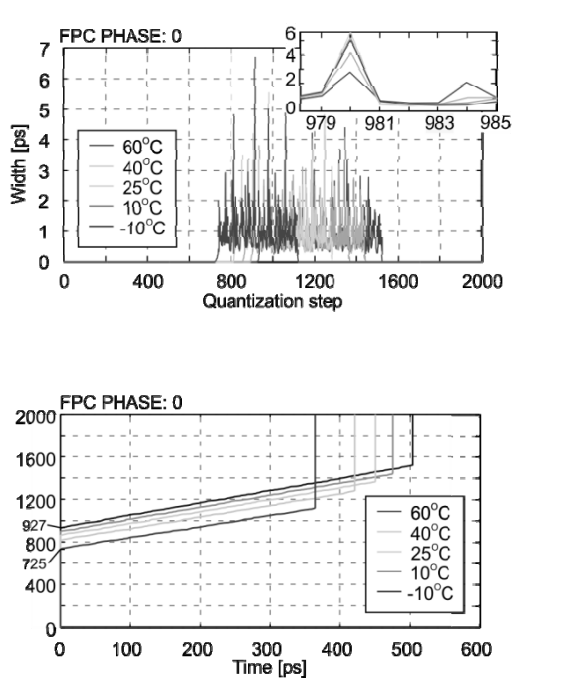

Fig. 3. a) Widths of the quantization steps, b) the transfer functions of SIS for the phase 0 of FPC in START channel evaluated in different temperatures

As expected, during the study we found that the quantization steps expanded with the increase in the temperature. If the ambient temperature increased by about 70°C, some steps increased their widths by approximately 50%, but some of them expanded even by 100%. For example, the width of the 980th step in −10°C is equal to 3 ps but in 60°C the width expanded to 6 ps. However, the fact that the changes in the FIS have a direct and large impact on the SIS is more significant than these width variations, because the width of the FPC segment determines the TDC measurement range. Based on the TDC transfer function for the phase 0 of the FPC, shown in Fig. 3b, one can state that the TDC range decreases with the temperature increase. This is consistent with the results presented in Section 3.

It can also be seen that the beginning of the active measurement range of the TDC is also changed. For the transfer function obtained at the temperature of −10°C, the 927th quantization step is the first active channel while at 60°C the first channel has the number 725. This significant change is primarily related to the increase in the propagation time of elements that are used in the construction of the TDC delay lines. However, it is also related to the delay of the buffer (Δt in Fig. 1b), which is responsible for intentional delaying of the START/STOP signal. A longer delay Δt, caused by the increase in temperature, results in the later appearance of the START signal in delay lines, which finally affects the quantization result.

Based on the results obtained from the tests, it is possible to evaluate the measurement inaccuracy due to the temperature changes. The inaccuracy is the result of discrepancies of characteristics, in other words, it occurs when the result of measurement is calculated based on a transfer function that is inadequate for the existing ambient temperature. The value of this inaccuracy is calculated according to the formula: $e = x_i - x^*_i$ where x_i stands for the value of the i^{th} quantization step of an unfitted transfer function, and x^*_i stands for the value of the i-th quantization step of the transfer function that matches the current temperature. The value of the measurement inaccuracy as a function of the number of the quantization step for various temperatures is shown in Fig. 4.

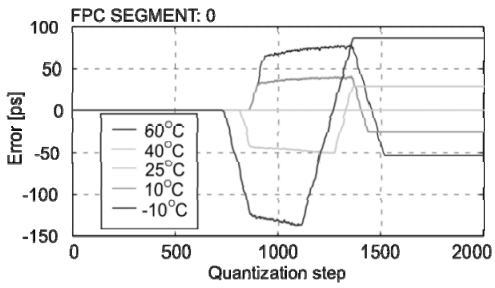

Fig. 4. Differences between the widths of quantization steps of the transfer function identified at temperature of 25°C and other selected temperatures

The transfer function obtained at the temperature of 25°C was taken as unfitted. The calculated value of the measurement inaccuracy (error) tremendously increases at the beginning of the quantization range but the further increase is moderate. The initial increase is caused by the change of the active range of the delay line, whereas the second is caused by the change of the propagation time of the elements used as delay buffers of discrete delay lines.

5. Summary

The results of the performed temperature tests allow stating that the changes in the FIS of the interpolation TC due to the drift of the ambient temperature have a greater impact on the measurement inaccuracy than the changes in the propagation times of the elements used as buffers of delay lines in the SIS. Such a large impact of the FIS on the measurement accuracy is mainly caused by the changes in the propagation time of the buffer B3 of the FPC generator. The simplest way to reduce the error appearing in the FIS is to limit the number of phases to two, e.g. 0° and 180°, by elimination of buffers B3, B2 and I2. However, two-fold reduction in the number of phases causes the necessity of extension of delay lines. The presented results of the tests allowed to assess the impact of the changes in the ambient temperature on both interpolation stages of the TC. The obtained conclusions are essential to develop a new method for elimination of the influence of changes in temperature on the measurement result that is the next stage of our research.

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