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Low Leakage and Robust Sub-threshold SRAM Cell Using Memristor

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***Abstract*—This work aims to improve the total power dissipation, leakage currents and stability without disturbing the logic state of SRAM cell with concept called sub-threshold operation. Though, sub-threshold SRAM proves to be advantageous but fails with basic 6T SRAM cell during readability and writability. In this paper we have investigated a non-volatile 6T2M (6 Transistors & 2 Memristors) sub-threshold SRAM cell working at lower supply voltage of VDD=0.3V, where Memristor is used to store the information even at power failures and restores previous data with successful read and write operation overcomes the challenge faced. This paper also proposes a new configuration of non-volatile 6T2M (6 Transistors & 2 Memristors) sub-threshold SRAM cell resulting in improved behaviour in terms of power, stability and leakage current where read and write power has improved by 40% and 90% respectively when compared to 6T2M (conventional) SRAM cell. The proposed 6T2M SRAM cell offers good stability of RSNM=65mV and WSNM=93mV which is much improved at low voltage when compared to conventional basic 6T SRAM cell, and improved leakage current of 4.92nA is achieved as compared.**

***Keywords*—6T SRAM cell; memristor; power dissipation; read and write operation; leakage current; stability; non-volatile circuit**

I. Introduction

MEMRISTOR was theoretically demonstrated by L.Chua in 1971[1] as a two terminal fourth passive circuit element after resistor, capacitor and inductor. In 2008, it was physically fabricated in HP labs [2] by using TIO2 nanoscale device. Due to its non-volatile characteristics, good scalability, low power consumption, high package density and the most important its ability to integrate with existing CMOS technologies, memristor can be used as memory and act as a strong candidate for future low power applications[3]. Power conscious design methodology can be considered as one of the important factors in recent researches for battery operated portable devices [3]. As technology is getting advanced, mobile applications requires and demands for low power consumption and low leakage current since unwanted power dissipation increases the temperature level of device and hence increases the probability of failure and reduces the lifetime of circuitry [4]. Therefore, scaling of supply voltages saves dynamic as well as leakage power. To reduce the power consumption in SRAM cell for low power application is a challenging task. Subthreshold operation is one of the technique to decrease the power consumption in SRAM cell where supply voltage applied is less than the threshold voltage of transistor [5] and utilization of this sub-threshold current is called sub-threshold conduction. Since the magnitude of current achieved in the sub-threshold region of operation is very less than the threshold region of operation, it takes higher time for charging and discharging the load capacitances which in turn decreases the speed of operation [6]. Transistor sizing is a technique which have significant impact on delay. If width of the transistor increases, delay can be improved but at the same time it dissipates more power. So, careful sizing of transistor is desirable for improving delay and preventing the trade-off between the parameters of the SRAM memory cell.

Researchers have already worked well at subthreshold voltages in SRAM cell and achieved good improvement in various parameters. Researcher have also worked on SRAM cell with memristor at VDD above threshold voltage. But, this work focusses on SRAM cell with Memristor (RRAM device-Resistive RAM-TIO2 –Titanium Oxide based) at subthreshold which is a new challenge and a new insight in the work done so far. Threshold voltage of PTM LP MOSFET model for 45nm technology is Vth0=0.62261V (NMOS) and Vth0=-0.587V (PMOS). The supply voltage discussed in the paper are 0.3V and 0.4V, which is well below the threshold voltage of the transistors, because of this reason we call all SRAM cells are operating in sub-threshold mode of operation. Basically, this work has combined the power reducing technique (subthreshold concept) with the memristor based SRAM cell to overcome the challenges faced in the conventional work by incorporating the non-volatile element (having an ability to store data even at power failure for definite time period) with CMOS technology (SRAM cell) in the subthreshold region and have achieved good performance characteristics which is discussed later.

Traditional basic 6T SRAM cell having a read and write failure as well as degraded SNM at low supply voltage, VDD [7] act a as key motivation of this work, then investigated SRAM based memory 6T2M (6Transistor 2Memristor) where Memristors are directly connected with supply voltage dissipates high power and change in memristance from HRS (high resistance state) to LRS (low resistance state) and vice versa is decided by flow of current through memristors. This paper proposes another memristor based SRAM cell where memrsitance change is controlled by node voltages

The rest of the paper is organized as follows: Section 2 gives a brief introduction on basics starting with 4T topology, subthreshold concept and memristor behaviour, Section 3

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explains 6T SRAM topology with and without memristor and a proposed circuit with their results and discussion, and finally section 4 concludes our work.

II. Brief Introduction

A. 4T2M SRAM Cell

In 4T2M SRAM cell explained in [8], one memristor is connected above each resistive load to make circuit more efficient and to reduce the disadvantages faced when simulated without memristor. In resistive load circuit of 4T SRAM cell, first problem is area. If we want good noise margin, then value of resistive load Rd must be high as shown in Fig. 1 and to implement very high value of resistance in VLSI circuit, very large area is required which is one of the major disadvantage. Second problem is that total power dissipation of 4T SRAM cell is high, since due to the presence of the resistance, current flow from VDD to VSS in resistive load having static power dissipation when cell transistors are ON. So, to eliminate the disadvantages faced, CMOS technology is used and moreover above that, usage of memristor proves to be advantageous in 6T SRAM cell than in 4T SRAM cell to obtain better results.

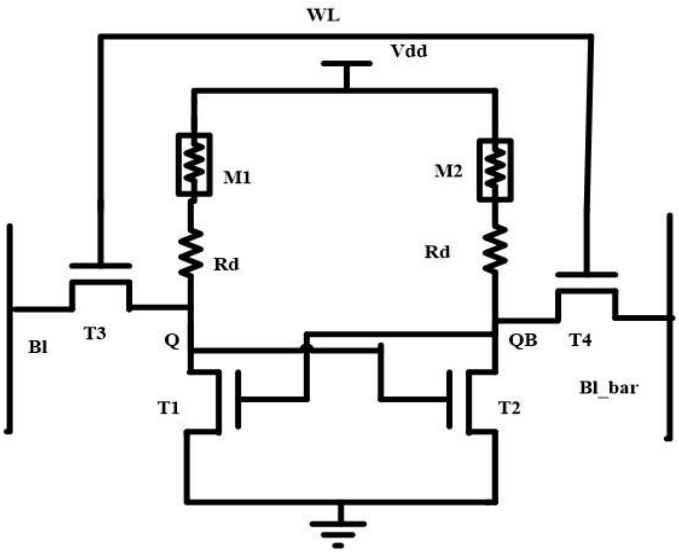

Fig. 1. Resistive load 4T SRAM cell using memristor

Memristor plays a vital role in the 4T SRAM cell, makes the cell non-volatile and also improves the overall quality. Memristor connected above resistive load is shown in Fig. 1 where M1 and M2 is connected in a similar way as described in [8] and resistivity change of memristor plays an important role. When memristors current is in forward direction, other memristors current will be in reverse direction, therefore, if memristor M1 is in High resistance state (HRS) then M2 goes in Low resistance state (LRS) and this mismatch in the resistivity of the memristor creates storage of the previous information. Another example for use of memristor in 4T SRAM cell is discussed in [21], where it is explained that memristor is a promising element helps in making a memory element with low power consumption and better read and write time.

B. Subthreshold SRAM cell

Normally SRAM consumes 40% of area, lot of power (even called as power hungry block). So, for ultra-low power application devices in 6T SRAM cell are operated in subthreshold conduction mode, where supply voltage is less the threshold voltage of MOSFETS [7]. The concept of subthreshold operation is suitable in areas where minimum power consumption is utmost requirement at lower supply voltages, application such as mobile applications, pacemakers and other battery-operated devices. It is very useful in circuits where system remains idle for longer period of time like in microprocessor and microcontrollers. So, in this work, it is successfully applied in memory cells to decrease leakage current and total power consumption. It saves leakage and hence total power consumptions but faced constraints which is minimized to a large extent in this paper. Many examples of SRAM memory cell successfully working with lower supply voltage is explained in [9]-[16] with one or other improved parameters.

C. Node Capacitance

Node capacitance is one of the important parameter to be taken care before working on any memory cell. There is a good impact on capacitance by using memristor in the cell. Since in this paper, our proposed work consist of memristor at both the nodes in symmetric pattern, there is no harm on capacitance value and is equal on both the sides. But it affects in the existing work [17] in which only one memristor is used in an asymmetric way disturbing the value of capacitance on both sides which is further improved by increasing the resistance of memristor and adjusting the values [17]. When large values (up to 1MΩ) of resistance is used in memory cell dominates the RC constant and timing for charging process of the nodes. So, timing waveform of each case further explains its effect. Being a symmetric circuit in the proposed work, low resistance values can also be used.

D. Memristor Characteristics, Physics and Parameters

Memristor is released as a thin semiconductor film sandwiched between metal plates where thin film consist of one insulating layer of TiO_2 and other oxygen deficient TiO_{2-x} layer. The doped layer TiO_{2-x} has lower resistance compared to undoped layer (TiO_2). Ionic mobility of oxygen vacancies are the reason behind change in resistance. The element can be said as resistor which is dependent on relative length of doped and undoped region of device. Hence, Memristance is used as digital device in this work by considering only the extreme values of memristance which is lowest and highest called as memristance states [18]. Polarity of device is decided by flow of current shown in Fig. 2, where state of memristor is explained to understand its behaviour. Fig. 2(a) explains low resistance state(LRS) (R_{on}) equivalent to logic '1' channeling the current through it with a forward biasing and on the other hand Fig. 2(b) explains high resistance state(HRS) (R_{off}) equivalent to logic '0' channeling the current in opposite direction in a reverse biasing. Therefore, memristance states can be altered high and low depending upon voltage polarity [19].

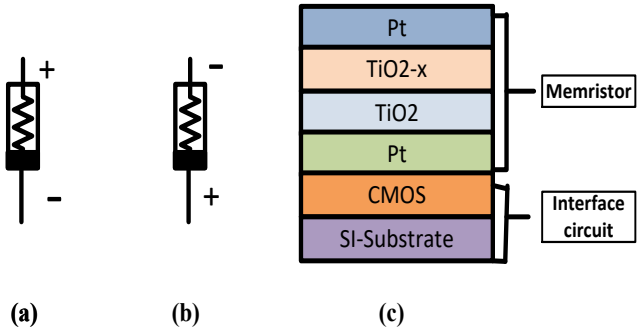

Fig. 2. (a)Low resistance '1'-Ron) (b)High resistance '0'-Roff (c) Memristor MOS layout for fabricartion[1][30][31]

Fig. 2(c) as mentioned in [20] explains the fabrication compatibility of memristor with CMOS technology. It illustrates Pt, TiO_2, and TiO_{2-x} layers onto the silicon substrate where thickness of TiO_2 is restricted below two nanometer to prevent conduction through individual layers separately. The Pt memristor wires are connected to the CMOS device on to silicon wafer. Electrical connections are made by photolithography and aluminum metal deposition [20]. So, fabrication of memristor is compatible with CMOS technology and takes less area when used in SRAM cell also discussed in [21].

The possible relationships between the fundamental quantities voltage, current, charge, and flux are given in [22].

$$dv = Rdi, \quad d\emptyset = Ldi, \quad dq = Cdv \tag{1}$$

Equation (1) provides the relation between resistor, capacitor, and inductor.

The memristor is said to be charge controlled if $\emptyset$=$\emptyset$(q). Then the voltage across the device is given by:

$$V = M(q) \tag{2}$$

Where M (q) is termed as memristance given by:

$$M(q) = \frac{d\emptyset(q)}{dq} \tag{3}$$

Equation (1), (2), and (3) is presented to understand the physics of memristor, the basic relationships is explained in [1].

Current-voltage relationship of memristor is defined as:

$$V = [M(x_1, x_2, \ldots\ldots x_n)][I] \tag{4}$$

Where, V defines voltage, I defines current and M is memristance which depends on x_n state variable. Memristance depends on frequency, applied input signal and parameter of window function for modelling non-linear boundary conditions.

Memristor SPICE model used in this paper is summarized in Table I is taken from [23] with change in memristance states values. Fig. 3 explains the basic I-V characteristics of memristor element which is a hysteresis loop. As explained the three fingerprints of memristor in [24], hysteresis loop shrinks to the linear line as frequency increases. It has its memristive behaviour until the hysteresis prevails. Fig. 3(a) tell the memristive behaviour at VDD =1V and f=400Hz, where Fig. 3(b) is at VDD =3V and 1kHz respectively. It is clearly observed that it shrinks to almost straight line when varied with frequency. Since this work is based on low voltage, memristor element should also show its characteristics at lower voltage. So, it is simulated at VDD=0.3V shown in Fig. 3(c), 3(d) and 3(e) at f= 1kHz, 5kHz and 20kHz respectively and it concludes that it can persevere its memristive effect at higher frequencies by using memristor parameters shown in Table I.

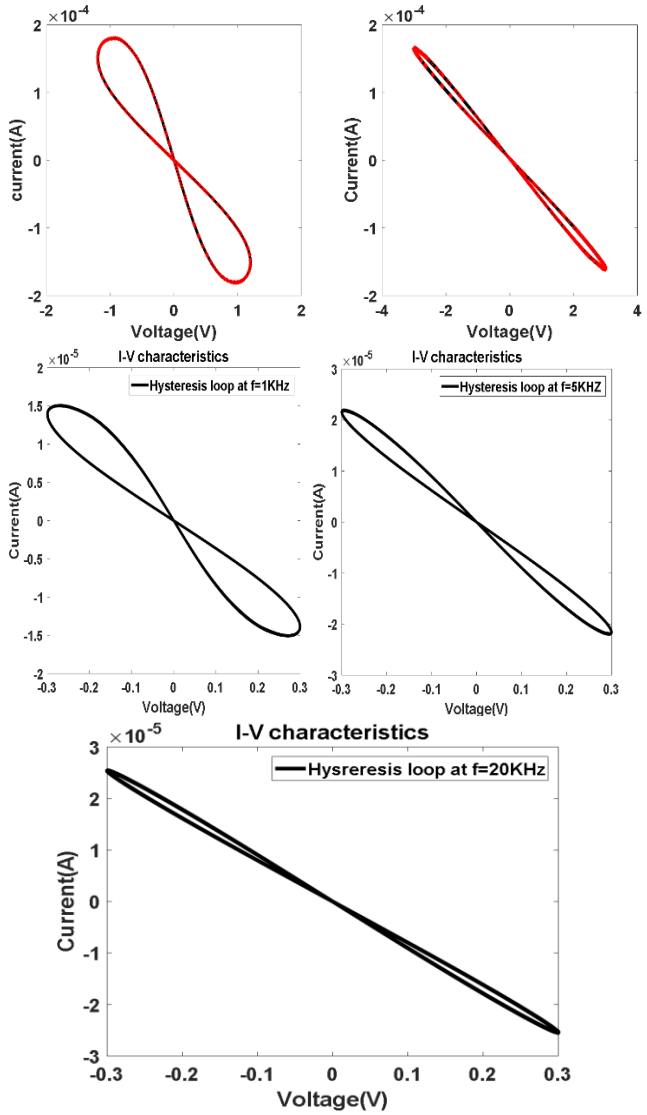

Fig. 3. I-V characteristics at (a) VDD=1V and f=400Hz (b) VDD=3V and f=1KHz(c)VDD=0.3Vand f=1KHz(d)VDD=0.3V and f=5KHz and (e)VDD=0.3V and f=20KHz

TABLE I
MEMRISTOR MODEL PARAMETER

Device parameter	Description	Magnitude
R_{on} (ohm)	Min memristance of memristor(LRS)	100k
R_{off}(ohm)	Max memristance of memristor(HRS)	1000k
R_{init} (ohm)	Initial resistance	11k
D	Width of thin film	10N
uv	Migration coefficient	10F
p	Parameter of the window function.	1

III. RESULTS AND DISCUSSIONS

This paper has worked on low voltage with memristor model discussed above in Table I with reduced power dissipation and leakage. Power consumption technique used is subthreshold concept seen in [9][12][13], leakage and delay is graphically

calculated from waveforms of simulated results as explained in [13][25] and [26] respectively. W/L ratio is taken as discussed in [27] and used 45nm PTM model [28] in this work of investigation.

A. 6T2M SRAM Cell at Subthreshold

SRAM cell do not require refreshing technique and it is absolutely volatile that means it stores data when power is supplied and loses data as supply is removed. The schematic of 6T SRAM cell is shown in Fig. 4, and its simulation is done using HSPICE software [29] at VDD=0.3V. Challenges faced by 6T SRAM cell at subthreshold region is that (1) by lowering the supply voltage, cell stability is decreased due to bad Static Noise Margin of the cell. For successful read, data stored at cross coupled inverter should not flip while maintaining the acceptable noise margin value and for successful write, data has to flip which fails in normal 6T cell, (2) Writability is also degraded badly because of process variations like temperature (3) Readability degradation makes impact on bit line leakage current and limits the total number of cells per bit line [12] [14].

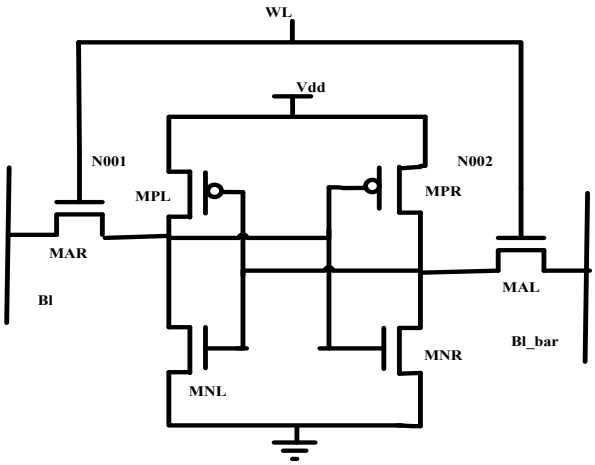

Fig. 4. Basic 6T SRAM cell

SRAM basically reduces the delay present between the processor and memories acting as cache memory and increasing the speed for input/output. Therefore, aggressive scaling of the devices and supply voltage drastically damages the SRAM cells when investigated with basic 6T SRAM cell. As seen in reference [7] [10][12]where operation of 6T is very challenging at low supply voltages and there is read and write ability degradation where optimization is very difficult at the same time. So, further SRAM cell using memristor is analyzed.

B. Memristor based 6T2M SRAM Cell at Subthreshold

Before discussing the proposed circuit, firstly we have investigated a memristor based 6T2M circuit as its adjusting structure is discussed in [30] [31] is evaluated at lower supply voltage VDD=0.3V, which is a new effort made to overcome the previous challenge. The architecture of 6T2M SRAM cell is shown in Fig. 5(a) in which both the memristors are directly connected to the supply voltage. It is then simulated and analyzed at subthreshold voltage to understand its behaviour when compared to previous case. Fig. 5(b) is the test circuit for the calculation RSNM/WSNM. Simulation results of read and write operation is explained in Fig. 6 and Fig. 7 respectively.

1) Write operation

Write delay is basically difference between wordline and written data on cross coupled logic. For writing in memristor based 6T SRAM cell, initially one of the bit lines are lowered depending on whether writing 0 or 1. Here, in Fig. 6, bit_bar is lowered to ground, it means, cell has stored '0' and writing '1' is to be done.

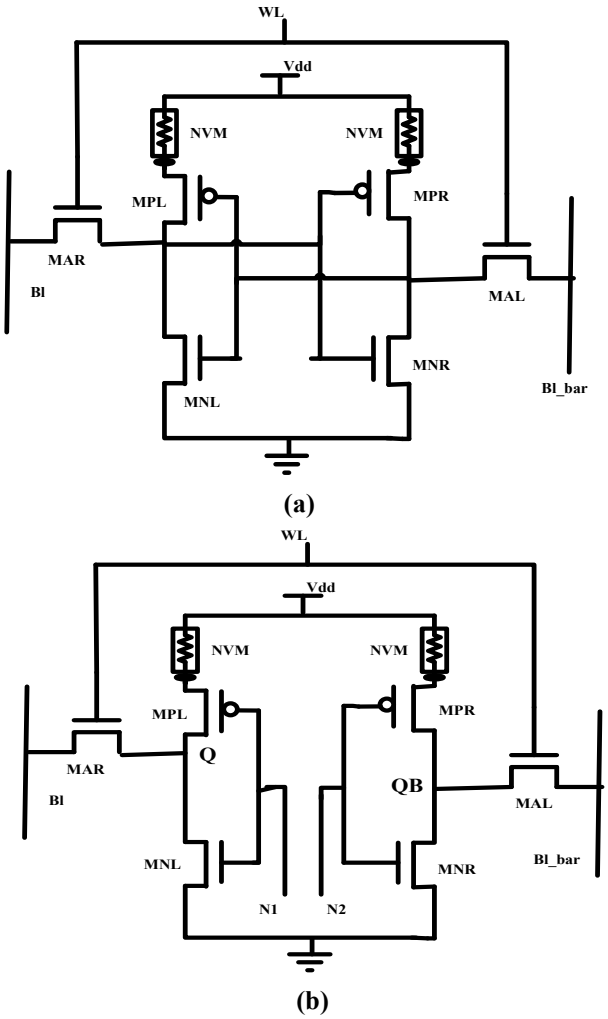

Fig. 5. (a) 6T2M [30] circuit evaluated at VDD=0.3V (b) Test circuit for calculating RSNM/WSNM

As the voltage rises by BL at node Q, current will sink to ground by MNL and node will be prevented for switching. Therefore, Q=0 and QB=1 is applied with VDD=0.3V, WL is high and memristor NVM is connected with direct power supply. It turns ON 'MAL' and current is drawn from QB to Bit_bar and memristor at right side reaches to HRS, and so, to prevent write failure, NMOS MAL should be stronger than MPR. In the same way writing 0 is done in which left memristor will reach the HRS. So, one of the memristor will HRS or LRS at a time. In Fig. 6, it is observed, though VQ and VQB has obtained waveform opposite to each other but the operating voltage is very less with supply of 300mV.VQB changes its state for 200mV whereas VQ changes its state for 50mV only.

Due to storage ability of memristor, although basic 6T2M is in working condition at low supply voltage which is better than conventional 6T SRAM cell in its behaviour and other performance parameter is calculated for the comparison.

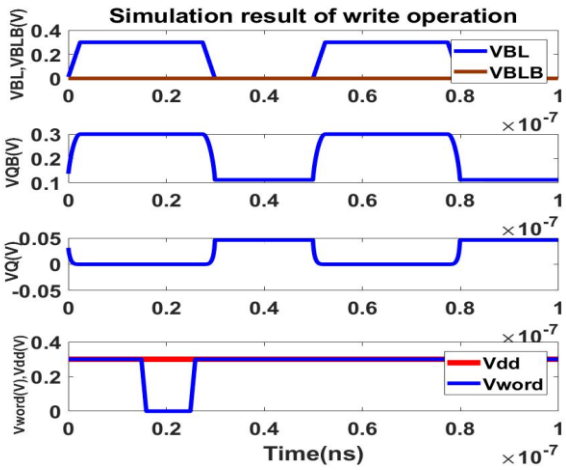

Fig. 6. Write simulation result of conventional 6T2M at VDD =0.3V

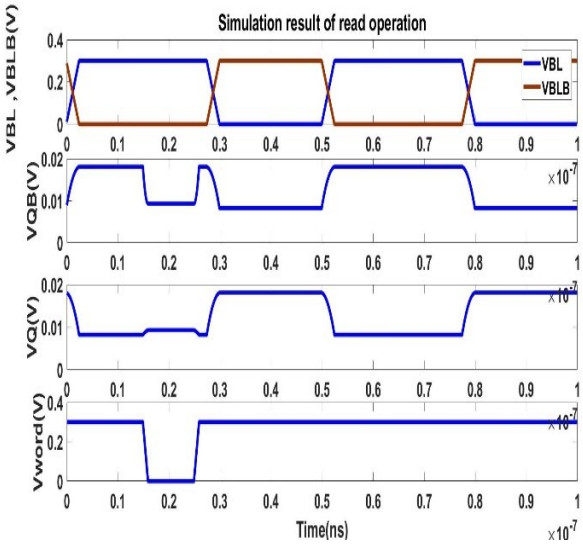

Fig. 7. Read Simulation result of 6T2M SRAM cell at VDD = 0.3V

2) Read Operation

For read operation, stored value needs to be evaluated and for that initially, both the bit lines are pre-charged to VDD which is 0.3V, WL is low, means both the access transistor MAL and MAR are disconnected from the cross coupled storage logic. If Q=0 and QB=1, means MNR and MPL will be OFF with right memristor in HRS. As memristor is having good storing ability at low voltage, it is storing some value helping to achieve switching operations. When WL is high, access transistors are high, releasing bit lines, voltage at VQ is same as bit_bar and no voltage transfer and no flipping occurs. Whereas at left side, capacitance would charge storage nodes and bit line remain unchanged, current would discharge from MNL to ground. To prevent read failure, MNL should be stronger than MAR. Behaviour of memristor is same as in write case. It is clearly observed in Fig. 7 simulation result, though node voltages are opposite to each other , change in operating voltage is very less at VDD=300mV where VQ and VQB changes for 10mV which is very small to detect other parameters.

Apart from other parameters, major disadvantage is seen in this investigation is that, power dissipation is very high due to direct connection of memristor with supply voltage which is improved further in the proposed structure discussed in the next section.

C. Proposed memristor based 6T2M SRAM cell

Proposed memristor based SRAM cell is shown in Fig. 8(a) with different configuration where one end memristor is connected to node voltages Q and Q_bar respectively and other end is connected to bit and bit_bar respectively. In this cell, memrsitance states are decided by the nodes of the SRAM cell without disturbing the main logic cell. In Fig. 5(a), since memristors are directly connected to supply voltage VDD, constant current flow through both the memristors directly increasing the power consumption of the overall circuit where as in the proposed circuit, connections are made in such a way, direct power supply is avoided as well as memrsitance state change from HRS to LRS and vice versa is maintained through node voltages Q and Q_bar during read/write operations decreasing power dissipation, leakage current and read/write delay to the greater extent. Fig. 8(b) is test circuit for calculating the SNM parameter. This proposed work has made effort in integrating the memristor model with basic 6T SRAM cell at scaled voltages which is a new insight done so far. There are other memristor based SRAM cell seen in [3][17][32][33] which explains the combinations like 7T1M, 8T2M, etc.

1) Read/Write Operation

During read operation, data has to be read from SRAM cell and to demonstrate the operation properly, proposed circuit is redrawn in Fig. 9 to understand the behaviour of the proposed circuit during the switching operation of read where in Fig. 9(a) both the memristors act as grounded and circuit works as a normal traditional 6TSRAM cell and memristors connected at nodes acts as storing element and supplies the stored previous data to the circuit from the node Q or Q_bar making it non-volatile in nature as this concept is also followed in [32]. The proposed circuit has maintained the Top and Bottom terminal of the memristor in such a way that both the terminals have same voltage by keeping BL and storage node equal and so there is no voltage difference, no polarity, no R_{on} and R_{off} (memristance states) and it behaves as a floating element just acting as storing element. It is already known that memristor can store information or previous data even when power is off with no voltage no current [22]. And so read operation of reading 0 or 1 is completed.. Its simulations result shown in Fig. 10, it is observed that node voltages operating in full range of 300mV with no distortions at supply voltage of 300mV which is better compared to previous case and performance parameters are discussed later in Tables.

During write operation, data has to be written in SRAM logic cell present at bit cells in the form of pre-charged bit cells, for obtaining this operation, input signal applied to bitlines BL and BLB in such a way that proposed circuit of Fig. 9 (b) will be fully active during write and from the simulation results shown in Fig. 11, it is observed that node voltages operating in full range of 300mV with supply of 300mV which is quite good.

In the Read/write operation of the proposed circuit, memristor connected directly to the nodes of the SRAM cell utilize all the advantages from the basic 6T SRAM cell and it

backs up the previous data maintaining the non volatility of the cell without any control line(CL) as bitlines (BLor BLB) only manages and shares with memristor to operate, it also reduces the area overhead.

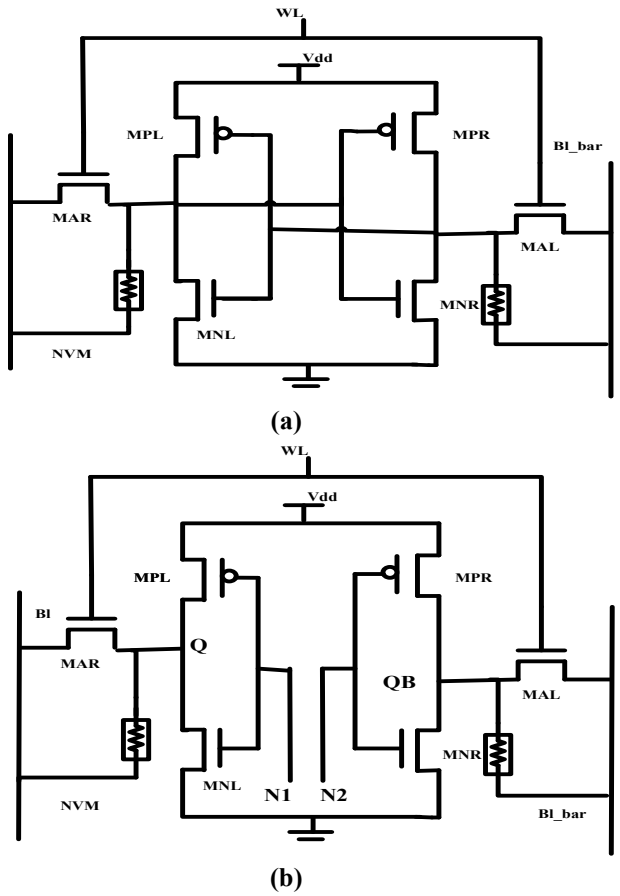

Fig. 8.(a) Proposed 6T2M SRAM cell (b)Test circuit for calculating RSNM/WSNM of the proposed Cell.

In store operation, basically, two sub operations SET and RESET are taken place which flushes the SRAM data into the memristor devices connected. In SET, both the bitlines are kept high so that memristor1(left memristor) is positively biased (if Q=0) making it LRS (low resistance state) and in RESET when both the biltlines are kept low, memristor 2(right memristor) is negatively biased(QB=1) and making it to a HRS (High resistance state). In this way, data are stored into the memristors.

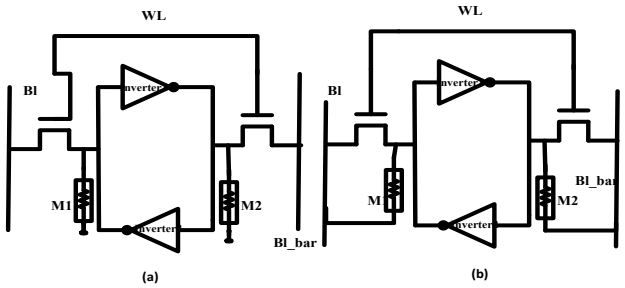

Fig. 9. (a) Behaviour of Proposed circuit during read operation (b) Proposed circuit during Write operation

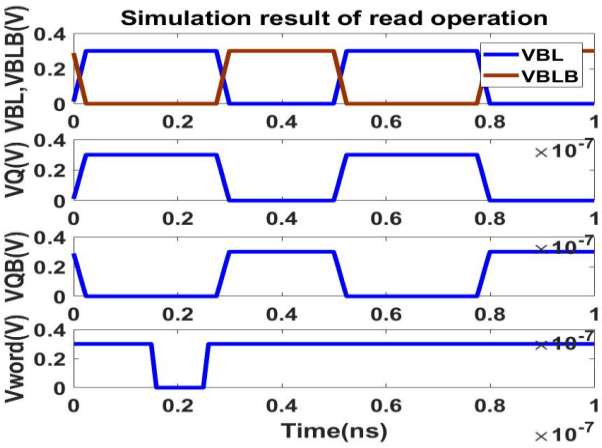

Fig. 10. Read simulation of proposed 6T2M SRAM cell

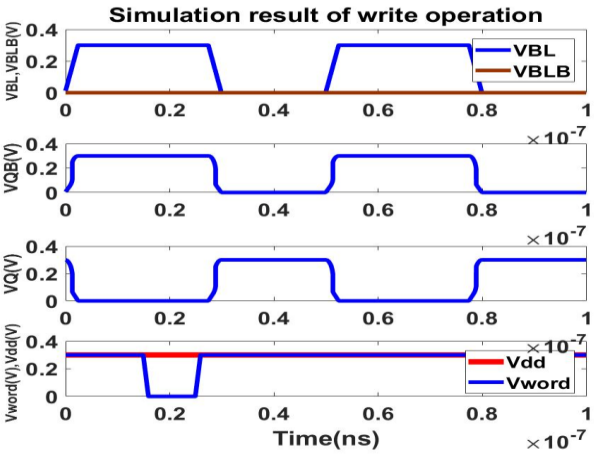

Fig. 11. Write simulation of proposed 6T2M SRAM cell.

During the restore operation of the proposed circuit, when power is OFF, i.e., VDD=0, Q and QB is forced to GND and when power is ON, data are collected from the memristors connected to storage nodes. Initially, in the power ON mode, both bit lines are kept low to ensure the node voltages VQ and VQB are at the same state and when supply gradually increases, both PMOS charges Q and QB with same rate and finally Q and QB discharges current though memristor respectively. The Value of the memristance depends on the memristance HRS and LRS and its polarity.

Power consumption and delay are improved in the proposed circuit effectively. We can say, this paper proposed a memristor based SRAM cell has caliber to inherit the advantages of 6T SRAM and having fast read and write operation even at low voltages using a non-volatile element. One of the best parts of this circuit is that, we do not require any extra control lines for memristors to control its operation because of its direct connection, thereby reducing area as discussed in [21]. Also, this connection reduces PMOS to access transistor ratio which reports for reducing write margin for further scope of work discussed in stability calculation.

D. SNM Calculation

1) RSNM (Read static noise margin) Analysis

RSNM quantifies the maximum amount of noise voltage which it can withstand at the internal nodes of the cell so that it does not flip the cell's contents. A noise voltage source is introduced between the nodes and is swept from 0 to VDD to obtain the voltage transfer characteristics (VTC) when both the access transistors nodes are pulled up to VDD as shown in test circuit shown in Fig. 5 (b) and Fig. 8 (b). A novel design of SRAM using Memristors at 45 nm PTM model where the voltage of the V(Q) node is plotted against that of the V(QB) node when the noise is introduced. On the same graph, the voltage swing of the V(QB) node is plotted against the V(Q) node. The maximum square fits within the VTC and the minimum of the two squares' side is the RSNM. Good RSNM defines good read stability [34]. Read Static noise margin (RSNM) is calculated is shown in Fig. 12 where RSNM is 58mV at VDD =0.3V and 70mV at VDD =0.4V respectively. These results are obtained from the VTC curve of test circuit in Fig. 5 where Memristor is connected between VDD and PMOS. In the same Fig. 12 also shows drawn the VTC curve of proposed circuit 6T2M from the test circuit shown in Fig. 8 (b) where memristor is connected between nodes and bit lines of memory cell and RSNM obtained is 65mV at VDD =0.3V and RSNM=80mV at VDD =0.4V which is quite good and improved when compared to both 6T conventional and previous 6T2M.

2) WSNM (Write static noise margin) Analysis

WSNM is obtained by the combination of read VTC and write VTC. This calculation is very sensitive since any error can flip the data and data is lost. This crucial parameter is difficult in subthreshold region but use of memristor improves it [30][31]. For writing 1 and 0 the width of smaller square which can be embedded between the lower half of curve is measured [17][34].Write static noise margin (WSNM) calculated is shown in Fig. 13 for the conventional 6T2M and proposed 6T2M SRAM cell with 130mV and 150mV respectively at VDD =0.4V obtained from test circuit in Fig. 5 (b) and Fig.8 (b). For good write ability, memory cell requires larger width of access transistor to keep pull up ratio lower value [7]. This criterion is maintained in memory cells using memristor with storing capability and achieves good WSNM when compared to non-functional 6T SRAM at subthreshold. Fig. 14 shows the WSNM of conventional and proposed 6T2M SRAM cells calculated from the same test circuit, the WSNM obtained is 60mV and 68mV at VDD =0.3V respectively. Its comparison is shown in Table II, for the analysis performed at VDD = 0.3V and 0.4V. WSNM is totally failed at subthreshold for 6T memory cell.

The WM (Write Margin) can be improved further in the proposed circuit by changing the resistance of Memristor during LRS (Low Resistance State) and HRS (High Resistance State). Memristance states do make changes in margin value [17]. This improvement was not possible in previous case (Fig. 5 (a)) because memristor is connected directly with VDD causing high power dissipation from the supply and so changing resistance state (R_{off}/R_{on},) can cause flow of higher current. But, in the proposed circuit, memristor is connected at nodes where resistance states can be changed and resistance is increased to check the WSNM which results in good write margin shown in Fig. 15 at VDD =0.3 and VDD =0.4. In the simulation result from HSpice tool, memristor model is used where high Roff/Ron ratio as explained in [19] and [35] is more beneficial and so various values of R_{off} are changed and kept R_{on} fixed, simulated and obtained various WM. In Fig. 15, when there is increase in VDD we can see there is a dip in the value, which is approximated because of architecture of the proposed circuit. As we further increase the value of VDD, there will be few dips and highs but however, at higher ratio, WM increases which we aim to. WSNM is further improved by increasing the Resistance states (R_{off}/R_{on},) from 10 to 100 where WSNM is 93mV at VDD =0.3v and 110 mV at VDD =0.4V. Table II shows the comparison of calculated SNM in this paper with existing circuits working at subthreshold voltage where proposed circuit has reached the level of 93mV which is much improved in terms of stability.

TABLE II
COMPARISON OF STABILITY WITH EXISTING CIRCUITS AT SUBTHRESHOLD VOLTAGE VDD=0.3V (WITH AND WITHOUT MEMRISTOR)

SRAM cells	RSNM(mV)	WSNM(mV)
6T[7]	24	Failed
6T2M[30]	58	68
6T2M (proposed)	65	75
6T2M(proposed with increased memristance value)	65	93
8T[10]	39.4	28.8
9T[13]	72	35
10T[10]	40.6	12.3
10T[13]	78	138

From the Figure 12 (b) it is concluded that, HSNM of the proposed circuit doesn't make much improvement even with the use of memristor when compared with the conventional basic 6T circuit at subthreshold voltage. HSNM of proposed circuit obtained is nearly 98mV at VDD=300mV.

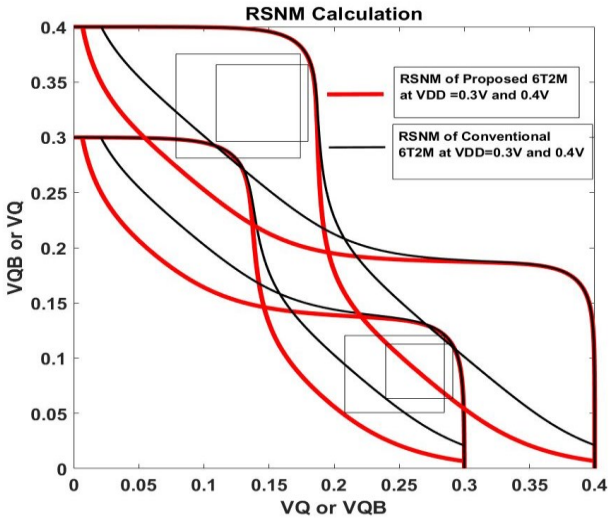

Fig. 12. (a) RSNM of 6T2M (conventional) and proposed 6T2M at VDD=0.3V and VDD=0.4V

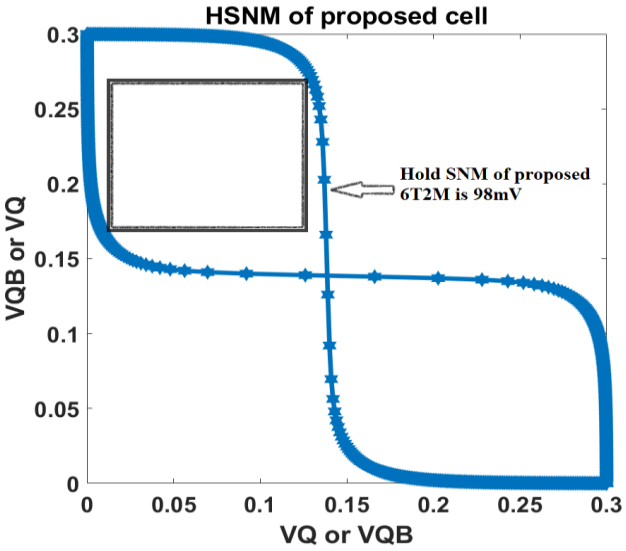

Fig. 12. (b) HSNM proposed 6T2M at VDD=0.3V

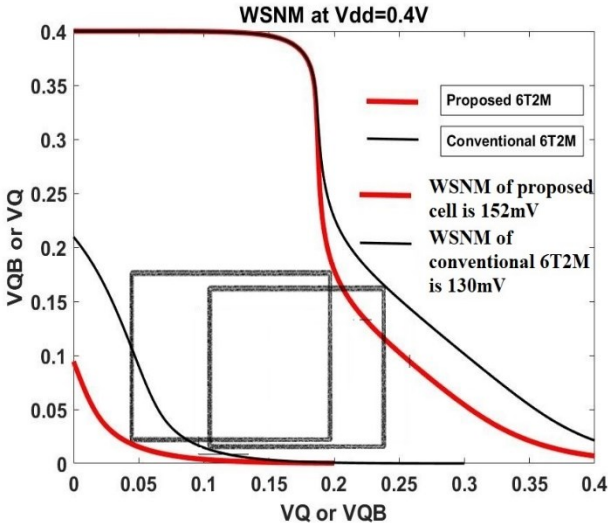

Fig. 13. Comparison of WSNM at VDD =0.4V

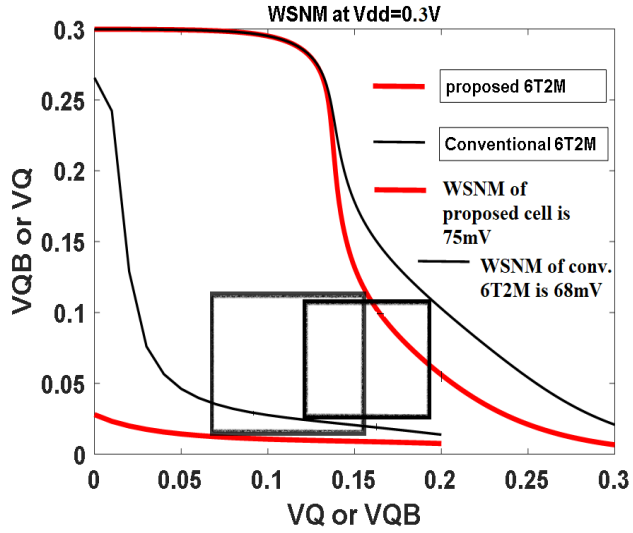

Fig. 14. Comparison of WSNM at VDD =0.3V

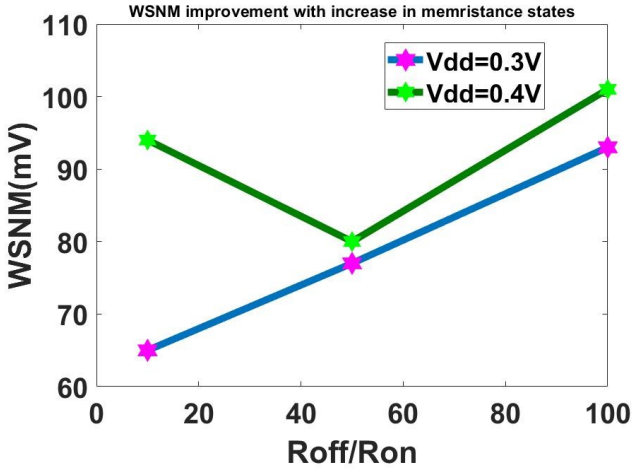

Fig.15. WSNM improvement with change in memristance

3) Delay and power

To be very specific, in this paper, at this very low voltage, time delay is increased with decrease in VDD and so there is sacrifice in speed of the circuit simulation. As VDD increases, time delay decreases and so speed increases [34]. Since working on subthreshold voltage, have to compromise with delay parameter in order to improve power and leakage. Although, if work is compared with various time delays at low voltage 0.3V, 0.4V etc. and compare with some existing work [14][5], this paper provides an improved time delay for basic 6T non-volatile SRAM cell comparatively.

Separate read and write power dissipation in the paper is a total power dissipation calculated due to the switching activity of the read and write operation. Static power in CMOS digital circuits is a result of leakage and static currents (the same sources which cause static energy). Dynamic power dissipation depends on the square of the supply voltage and linearly on the frequency ($P = CV2\,f$), if both the supply voltage and frequency are scaled down, there is a cubic reduction in power consumption.

E. Leakage Calculation

The leakage current is one of the major factors responsible for the power consumption in the SRAM cell [11][13]. Different components of leakage currents in SRAM cells are subthreshold leakage current (Isub), gate leakage current (Igate) and junction leakage current (Ijn) [25]. Ideally, during a standby mode of SRAM cell, the unwanted flow of current is leakage current which flows in different situations consumes more power. Hold failure occurs when the leakage current rises in the pull down transistor connected to node storing '1'. As technology is further scaled, supply voltage applied is becoming lower, so leakage increases and node storing value 1 reduces from VDD, if this VDD becomes lower than trip point of voltage containing 0, then cell flips causing hold failure. Improving this require high threshold of pull down transistor disturbing other SRAM metrics. There should be a balance of trade off caused between smaller areas, minimum power consumption by reducing supply voltage, faster read and write ability and leakage current. Since memristor does not take much space/area as mentioned in [21] with value of about 0.000196 µm2, which is less than that of the

PMOS transistors used. So memristor does not have negative impact on leakage current.

Apart from this, 6T2M (Fig. 5) suffer from higher leakage due to the existence of direct path from the memristor device to the ground. But leakage current of proposed circuit (Fig. 8) is less compared to conventional 6T2M because its path connects the memristive device to the storage node Q or QB with higher memristance state at the same time. It means, memory cell always have one memristor in HRS which decreases the leakage current almost by 80-90% when compared to 6T2M. Table III shows the comparison of leakage current, where it is observed that the proposed circuit have quite less leakage current. Table IV shows the comparison of SRAM topology with and without memristor at sub-threshold for delay, power consumption, Stability and leakage current, where it is observed that in sub-threshold region of operation 6T2M (proposed) is giving the best results in terms of discussed performance parameter. After analysis and simulations done, results obtained from HSPICE concludes with comparison as explained in Table II, III and IV in which traditional 6T, 6T2M adjusting and Proposed 6T2M SRAM cells are compared at VDD=0.3V, where it is reported that power consumption is quite improved, read delay and write delay are maintained comparatively and also assures memory stability by calculating its SNM (Static Noise Margin) and leakage current during standby mode as well as during the switching mode.

TABLE III
COMPARISON OF LEAKAGE CURRENTS OF EXISTING WORK WITH AND WITHOUT MEMRISTOR

Parameter	Leakage currents
8T(0.3)[13]	7.42nA
10T(0.3V)[10]	4.13nA
7T1R(0.8V)[17]	10nA
8T2R(0.4V)[32]	25uA
6T(0.3V)[7]	10.6uA
6T2M(0,3V)[30]	110nA
6T2M(0.3V)[proposed)	4.92A

TABLE IV
COMPARISON OF SRAM TOPOLOGY WITH AND WITHOUT MEMRISTOR AT SUB-THRESHOLD FOR DELAY, POWER CONSUMPTION, STABILITY AND LEAKAGE CURRENT AT VDD= 0.3V

Parameter	Performance characteristics	6T[7]	6T2M[30]	6T2M proposed
1.Delay	Twrite	Fails	540ps	242ps
	Tread	Fails	494ps	432ps
2.Power	Pwrite	Fails	0.930uW	0.182uW
	Pread	176.36uW	0.803uW	0.528uW
3.SNM	RSNM	24mV	58mV	65mV
	WSNM	Failed	60mV	93mV
4.Leakage current		10.6uA	110nA	4.92nA

CONCLUSION

In this work we have successfully investigated the memristor based SRAM cell 6T2M (6 transistor 2 memristor) at sub threshold region with supply voltage VDD=0.3 where memristor is directly connected to the supply voltage which consumes higher energy but SRAM cell functions well which has failed in traditional 6TSRAM cell at sub-threshold. This work also proposed another SRAM cell with different connection of memristor which avoids direct connection of supply voltage and change in memrsitance states is controlled by node voltages of SRAM cell without disturbing the logic cell at VDD=0.3 results in improved power dissipation, read delay, write delay, better SNM and less leakage current. However, at subthreshold region, speed of the circuit is the biggest sacrifice and so its performance is limited to ultra-low applications, but memristor usage specially in the proposed circuit it has improved the speed by larger extent. So, as per the results achieved, it is concluded that memristor based SRAM cell is a good candidate for subthreshold application than simple 6T SRAM cell.

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