Design Considerations for an 8-decade Current-to-Digital Converter with fA Sensitivity

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***Abstract*—Radiation measurements for high energy physics experiments, nuclear facilities, hospitals and hadron therapy institutes require precise low current sensing. This paper provides a methodology for experimental characterisation of the leakage current sources present at the input of a current-to-digital converter. The limitations in sub-picoampere current measurements are presented along with the design of an ASIC that can accurately measure currents in the femto-ampere range after integrating over sufficient time. Proposals to minimise the subthreshold leakage current of the switches connected to the input, the leakage current of the package, the leakage of the PCB and the leakage related to the ESD protection diodes are shown. The remaining leakage current can be measured and subtracted. The front-end can digitise currents over 8 decades produced by a radiation detector. These guidelines were established during the current design and testing and will be used for the second version of the front-end electronics that will be installed at CERN for radiation protection and monitoring.**

***Index Terms*—Radiation monitoring, ultra-low current sensing, leakage currents, sub-picoampere current measurements**

I. Introduction and Motivation

IONISING radiation measurements for radiation protection and beam diagnostics in hospitals, require very wide dynamic range and at the same time ultra-low current sensing starting from the femto-ampere range. The leakage currents and the measurement procedure are critical for current measurements starting from that low range. This research was initially performed in order to provide CERN's radiation protection group with an ASIC front-end able to be connected to an ionisation chamber detector and measure ultra-low radiation levels, because of the stringent legislation in matters of radiation protection for personnel and environmental safety. By the constant monitoring of the ambient radiation dose in many areas in and around CERN's sites, the public and personnel will be protected from any unjustified exposure to ionising radiation.

The main limitation in a system that is capable of measuring currents starting from fA up to μA is the leakage currents in the input of the front-end that are comparable to the signal to be measured. This is the motivation for the Ultralow picoammeter (Utopia 1) ASIC that is presented here. The limitations in measuring ultra-low currents and the methodology that was followed in order to estimate the different sources of leakage current values, minimise them or compensate for them and successfully measure the lowest possible input current on-chip are presented. The Current to Frequency Converter (CFC) used as a testing structure to characterise the leakages will also be used to digitise the currents produced by the detector over 8 decades.

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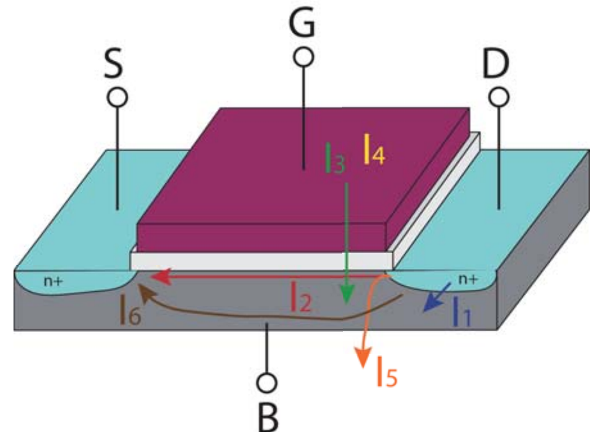

Fig. 1. Leakage current mechanisms in an nMOS transistor

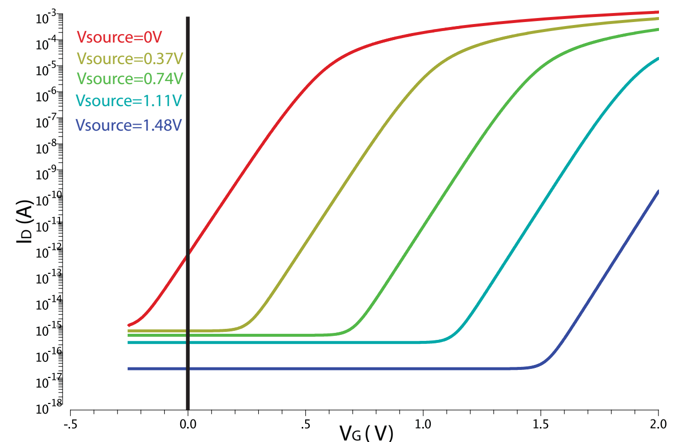

Fig. 2. Drain current versus gate voltage for an nMOS transistor of W/L=1/0.35 for different source voltages

II. Sources of Leakage Currents

The leakage current mechanisms for a MOS device are presented in [1]. For short channels these are shown in Fig. 1 and are the reverse bias p-n junction leakage I_1, the subthreshold leakage I_2, the oxide tunneling current I_3, the gate current due to hot-carrier injection I_4, the Gate-Induced Drain Leakage (GIDL) I_5 and the channel punchthrough current I_6.

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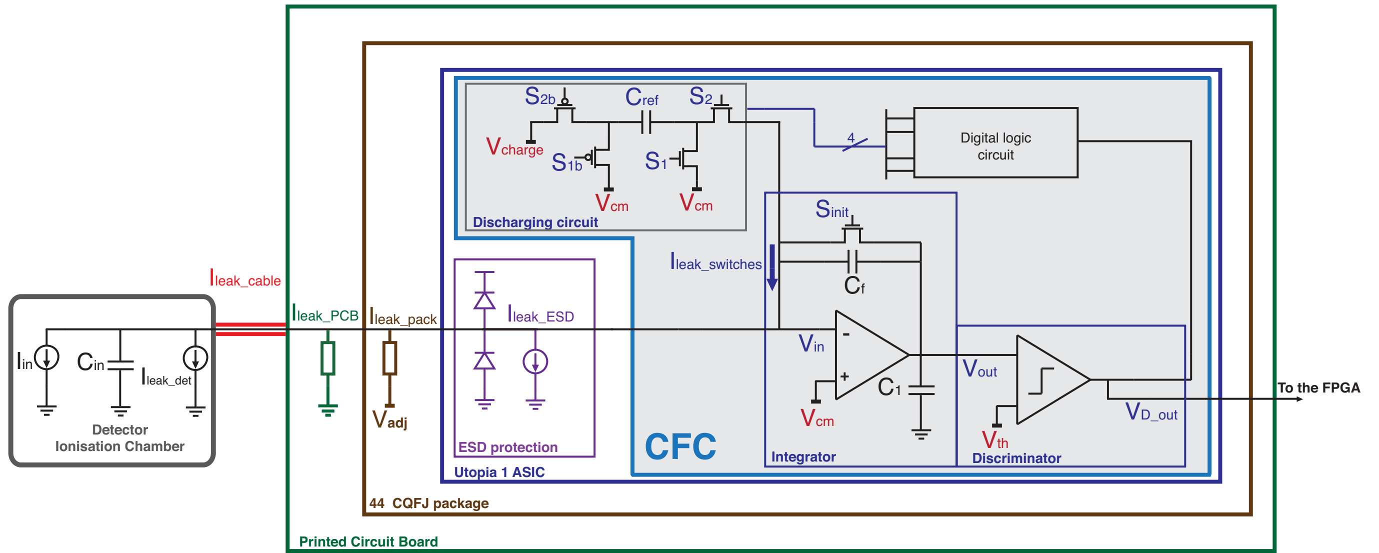

Fig. 3. System architecture of Utopia 1 ASIC including sources of leakage current

Regarding the technology, AMS 0.35 μm demonstrates better performance in terms of subthreshold leakage and substrate leakage currents compared to the newer technologies of 0.18 μm and 0.13 μm and this is why it was selected for this development. The dependence of the leakage current mechanisms on technology scaling and on temperature are explained in [2].

The subthreshold or weak inversion leakage current is the dominant leakage current source and for a minimum size transistor in 0.35 μm technology is in the order of hundreds of fA. Afterwards, the reverse diode leakage current of the drain or source of a minimum size transistor is around 10 aA [3]. Due to the thick gate oxide of the technology and the smaller values of the other leakages that are beyond the scope of this research, the other leakage mechanisms could be neglected.

One equation that describes the drain current in weak inversion is [5]:

$$I_{DS} = \frac{W}{L}\hat{I}\left(V_{GB}\right)\left(e^{-V_{SB}/\varphi_t} - e^{-V_{DB}/\varphi_t}\right) \quad (1)$$

where

$$\hat{I}\left(V_{GB}\right) = \mu\frac{\sqrt{2q\epsilon_s N_A}}{2\sqrt{\psi_{s\alpha}\left(V_{GB}\right)}}\phi_t^2 e^{[\psi_{s\alpha}(V_{GB})-2\phi_F]/\phi_t} \quad (2)$$

and ϕ_t is the thermal voltage, ϕ_F is the Fermi potential, $\psi_{s\alpha}$ is the surface potential, and $\sqrt{2q\epsilon_s}$ has a value of $5.8\cdot10^{-16}C\cdot V^{-1/2}\cdot cm^{-1/2}$ for silicon.

One method to decrease the subthreshold leakage current is to drive the gate G to a voltage outside the existing rail voltages. A better alternative is the source shifting technique as explained in [3], where the subthreshold current can be reduced by increasing the V_{SB} and connecting the source to a different potential relative to the bulk. Then the whole range down to the diffusion diodes reverse leakage is exploited.

A simulation of this is depicted in Fig. 2 for different source voltages starting from 0 V and sweeping up to 1.48 V. The drain voltage is at 1.65 V. The disadvantage of increasing V_{SB} is that this also reverse biases the drain to bulk diode and increases the diode leakage. That increase though, proved to be negligible for the currents of interest (fA). An alternative solution is given in [4] where a pMOS transistor in a well allows the bulk voltage to differ from the substrate voltage.

The architecture of the Utopia 1 ASIC and the leakage current sources are presented in Fig. 3. For decreasing the subthreshold leakage, $I_{leak_switches}$, of the switches that are connected to the input, the source shifting technique is used. The common mode voltage V_{cm} of the amplifier is at a different potential relative to the ground and this allows indirect control of the source voltage of the nMOS switches S_2 and S_{init}.

The reverse bias leakage current of a p-n junction is given from:

$$I_{DB} = -I_S\left[e^{-V_{DB}/V_t} - 1\right] \quad (3)$$

The reverse current magnitude is strongly dependent on temperature, doubling for every 10^oC increase of it. The reverse diode leakage is dependent on junction geometry and as such is small enough to be neglected for the source/drain of the transistors in the input stage of the circuit. The same is not true for that of the protection diodes, I_{leak_ESD}. This is one of the most critical parameters for this application and is investigated in the measurements section.

Lastly, another source of leakage current is the leakage coming from the external connections to the package I_{leak_pack}, the printed circuit board (PCB) I_{leak_PCB} and the cable I_{leak_cable}. These sources of leakage should be also taken into consideration during the design of any system measuring low currents.

III. Utopia 1 Design

A. Operating principle

The Current to Frequency Converter (CFC) that is presented in Fig. 3, is used as the front-end in order to digitise currents

over a wide dynamic range that are generated from a current source. Other systems that use similar working principles are presented in [6], [7], [8] and [9]. However, the lowest current that these systems were able to digitise is limited to 300 fA. As depicted in Fig. 3, an integrator with a feedback capacitance C_f integrates the input current, I_{total}, including the I_{in} and the sum of leakages I_{leak} and provides an output voltage, V_{out}, that is compared with a voltage threshold, V_{th}, by a discriminator. When the V_{th} is crossed, a fixed amount of charge that ideally is $Q_{ref} = C_{ref}V_{ref}$ where $V_{ref} = V_{charge} - V_{cm}$ is injected into the input through a stray insensitive switched capacitor discharging circuit to discharge the C_f. By observing the V_{D_out} and counting how many times the charge injection circuit is activated in a measuring time window, T_w, the input current can be measured.

The ideal number of counts is given by:

$$N_{counts_ideal} = \frac{I_{in}T_w}{C_{ref}V_{ref}} \tag{4}$$

B. Reference charge

For an op-amp with finite GBW the actual reference charge value is:

$$Q_{ref_actual} = C_{ref}V_{ref} - C_{ref}\Delta V_{in}(t) \tag{5}$$

where $\Delta V_{in}(t) = V_{in}(t) - V_{cm}$.

At the end of the Q_{ref_actual} transfer, the $V_{in}(t)$ is not V_{cm} because of the ramping of the V_{out} due to the I_{in}. At the end of the discharge, the value of the ΔV_{in} is given by:

$$\Delta V_{in}(t) = \frac{-I_{in}}{C_f} \cdot \frac{1}{\beta_f \omega_u} \tag{6}$$

where $\omega_u = 2\pi GBW$, C_{in} is the capacitance of the detector and β_f is:

$$\beta_f = \frac{C_f}{C_f + C_{in} + C_{ref}} \tag{7}$$

The real number of counts in the measuring time window T_w is given from:

$$N_{counts_real} = \frac{I_{in}T_w}{C_{ref}V_{ref} + \frac{C_{ref}}{C_f}\frac{I_{in}}{\beta_f \omega_u}} \tag{8}$$

A numerical example with I_{in}= 1 μA, C_{ref}= 1 pC, C_f= 1 pC, V_{ref}= 1 V and T_w= 100 ms is given in Fig. 4, where the effect of the GBW is presented compared to the ideal case. For this simulation, the capacitance of the detector is considered to be C_{in}= 50 pF, which is the worst case between the two available commercial detectors that are used in this work. When the second detector is used where the C_{in}= 9 pF, the error in the high input range is alleviated.

The dynamic range in the lower end is limited because of the leakage currents and in the upper end because of the bandwidth limitations.

The upper current limit is given by:

$$I_{max} = \frac{Q_{ref}}{T_{charge} + T_{discharge}} \tag{9}$$

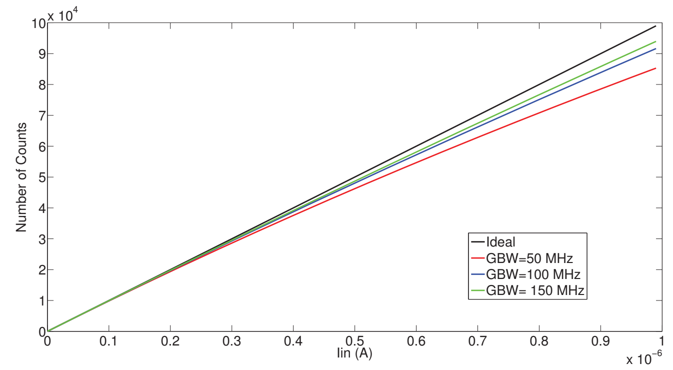

Fig. 4. Simulation of input current versus number of counts for different GBW values

TABLE I
SUMMARY OF UTOPIA 1 ASIC CHARACTERISTICS

A/D Converter	Technology	AMS 0.35 μm
	Power Supply	3.3 V
	Clock	10 MHz
	Die Size	2.6 mm x 2.6 mm
	Polarity	Negative with this biasing
	Number of Channels	4
	Time Window T_w	100 ms
Integrator	A_0	86 dB
	GBW	100 MHz
	ϕ	62 deg
	C_f	1 pF
	V_{cm}	1.5 V
	V_{th}	2.5 V
Discharging Circuit	C_{ref}	1 pF
	V_{ref}	1 V
	Q_{ref}	1 pC
	V_{charge}	2.5 V

In the upper end, the measuring time window T_w is set to be 100 ms for currents over 10 pA but in the lower range it needs to be increased, since lower radiation implies lower I_{in} and this requires a longer integration time to reach the point where the integrator output exceeds the comparator threshold.

The integrator that was designed for the ultra-low current sensing is a two-stage Miller amplifier with pMOS input differential pair for lower 1/f noise. The discharging circuit is a stray insensitive switched capacitor circuit. The summary of the front-end characteristics is shown in Table I. The ionisation chambers are biased to produce negative current and this is the reason why the architecture was initially built unipolar.

C. Design modifications for leakage current measurements

Four channels were implemented to test different variants and measure independently each leakage current source. The voltages V_{cm}, V_{charge} and V_{th} and the initialisation signal S_{init} are common for all the channels. The clock can be provided either by a 10 MHz oscillator on the test PCB or by an external source.

The differences between the channels CH1, CH2, CH3 and CH4 are summarised in Fig. 5, marked as (a), (b) and (c) and are explained below.

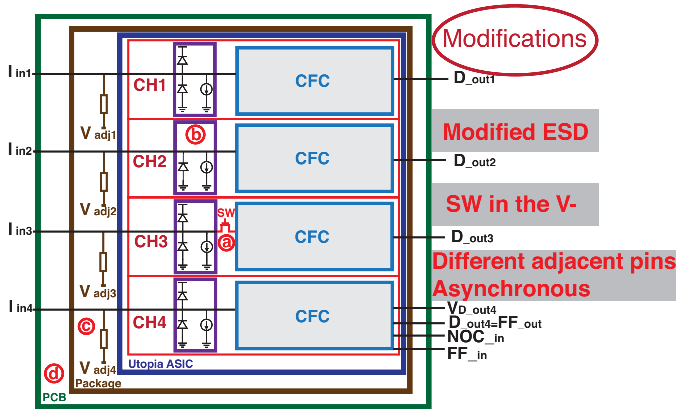

Fig. 5. Block diagram of the four channels of Utopia 1 ASIC

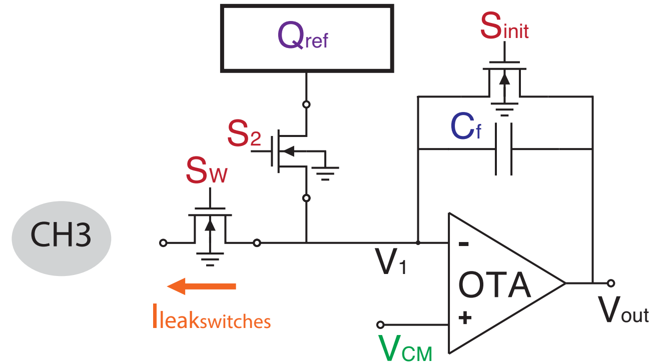

Fig. 6. CH3 test structure to measure subthreshold leakage of the switches

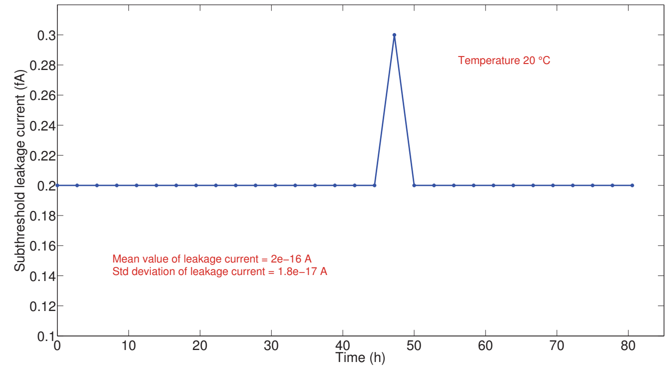

Fig. 7. Mean value of subthreshold leakage for CH3

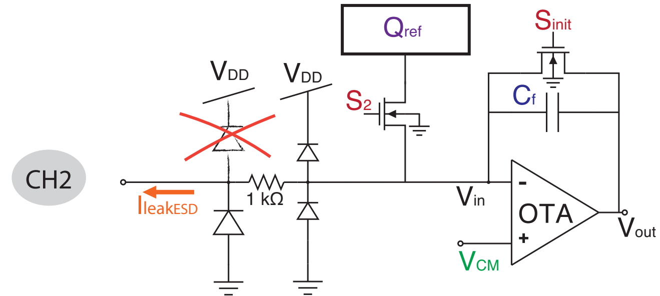

Fig. 8. CH2 test structure to measure ESD protection leakage current

The CH1 was implemented with normal ESD protection. The ESD protection of CH2 was modified and the upper diode of the standard library cells was removed as can be seen in (b). That way the effect of the ESD protection leakage current can be estimated. The CH3 has normal ESD protection but an nMOS switch was put in the input as seen in (a), in order to isolate the diodes and the package from the integrator input. The subthreshold leakage current of the switches that has already been eliminated due to the bulk effect can be measured. Finally, the CH4 has the same input structure as the CH1 but different adjacent pins. The effect of the external leakage currents related to the package potential can be measured with this structure. In CH4, the asynchronous operation could be also checked, since the discharging circuit could be managed externally.

IV. Measurement Results

A data acquisition system based on Spartan-6 LX9 MicroBoard and NI LabVIEW software was developed and connected to the digital output V_{D_out} of the ASIC. The following measurements were performed in a climatic chamber, where the temperature and the humidity were controlled. Since fA measurements are very delicate, the testbench was carefully designed and the PCB was put inside a metal box to be shielded from interference.

A. Leakage currents

In order to identify each leakage current source, multiple measurements were performed with the four channels of the ASIC in different steps. The leakage current could be measured directly when the input was open and the system was free running. In order to measure sub-picoampere currents, the measurement time should be sufficiently increased and more samples should be acquired for better statistics. The system is designed to accept negative input currents. When the polarity of the leakage current is positive, it can be measured indirectly if a small input current is injected into the input and the perturbation from the expected value is estimated by observing the number of counts [9]. The different sources of leakage currents are analysed in the following subsections.

1) Switches in the input: at the beginning, the subthreshold leakage current $I_{leak_switches}$ of the switches connected to the input SW, S_{init} and S_2 was measured as shown in Fig. 6. If the nMOS switch in the input of the CH3 remains open, the integrator's input is disconnected from the PCB, the package and the ESD protection. As depicted in Fig. 7 the $I_{leak_switches}$ is below 1 fA with an acquisition time of 82 hours. To achieve such a low value for the subthreshold leakage, the source shifting technique was used and the common mode voltage V_{cm} was set to 1.5 V, a value that increases the threshold voltage of the transistors.

2) ESD protection: after the subthreshold leakage current elimination by using the source shifting technique, one of the main leakage current sources is the ESD protection. In order to test the behavior and the leakage related to the protection diodes, CH2 was implemented as shown in Fig. 8. Different leakage current behavior was observed because of

the ESD protection differences between CH1 and CH2. The leakage current values for these two channels as a function of time are presented in Fig. 9. The CH1 that has the standard ESD protection exhibited leakage current of different polarity according to the selected V_{cm} value. The decrease in the leakage current according to the selected V_{cm} can be observed in Fig. 10, where the leakage current of CH1 at 10^oC is plotted as a function of V_{cm}. When the V_{cm} was set below 1.55 V the current changed polarity. On the other hand the CH2, where the biggest ESD protection diode that is connected to V_{DD} was removed, exhibited only negative leakage current that could be directly measured with the CFC. The I_{leak_ESD} leakage current values were stored and could be used for compensation when currents are injected through a laboratory instrument.

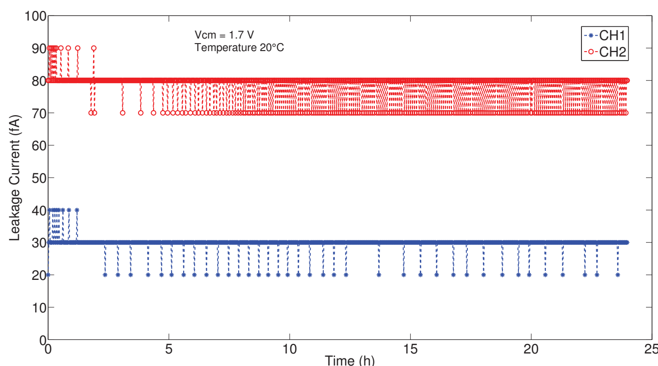

Fig. 9. Leakage current as a function of time for CH1 and CH2

3) Package and adjacent pins: the different voltage on the pins adjacent to the measuring channel is another potential source of leakage current and that was observed when the bondwires were disconnected. It was also evident when measuring CH4 (connected initially to pin 8) that has V_{DD} as one adjacent pin and it demonstrated high leakage current of +120 fA. When the bondwires were removed and CH4 was bonded back as shown in Fig. 11 to pin 4, the leakage current was measured to be +14 fA at the same V_{cm}. However the polarity of the leakage was opposite compared to CH1 that had ground as adjacent pin. As a guideline, guard rings should be used and a triax cable should connect the ionisation chamber to the measuring channel in order to eliminate the leakage currents related to the package.

4) PCB: the PCB that hosts the ceramic package with the ASIC was implemented without any ground plane under the inputs for better insulation. The leakage current of an ASIC with a cable connected to the input was measured over a long time and then the same test was repeated with the PCB disconnected from the chip. The PCB leakage I_{leak_PCB} proved to be extremely low compared to the other sources of leakage current.

B. Temperature dependence of the leakage current

In Fig. 12, the input of the CH2 was disconnected from the package, so the leakage is mainly related to the ESD protection reverse bias current and doubles with a temperature increase of 10^oC as expected. The temperature of the ASIC was also measured with an infrared camera and it was at most

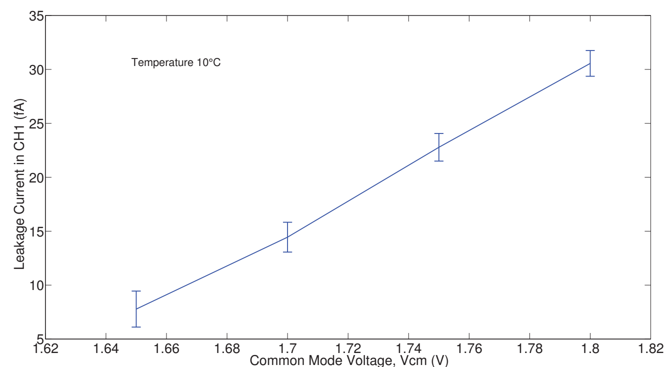

Fig. 10. Mean value of leakage current versus common mode voltage

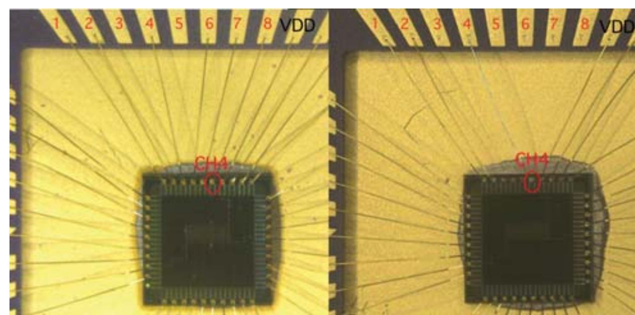

Fig. 11. Difference in CH4 bonding

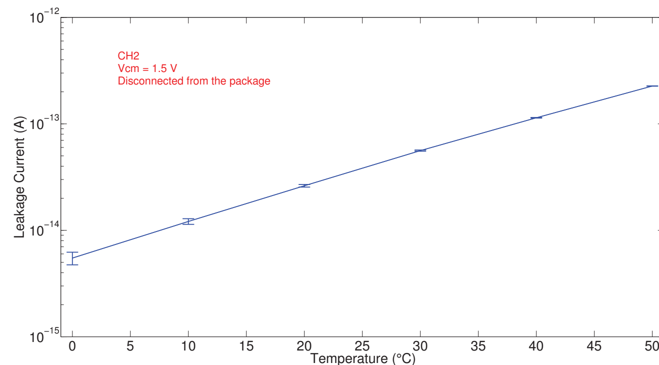

Fig. 12. Mean value of ESD protection leakage current of CH2 versus temperature

2^oC higher than the temperature in the climatic chamber. For sub-picoampere current measurements the temperature of the environment should be kept constant.

C. Leakage current compensation

After measuring the leakage currents, the performance of the Utopia 1 ASIC was studied at a constant temperature of 20^oC using a precise laboratory current source from Keithley. The mean absolute value of the measured current after compensation and also the ideal curve are presented as a function of a testing current in Fig. 13 for CH1 and Fig. 14 for CH2, for currents starting from -50 fA up to -500 nA. The absolute error is less than $\pm$ 2.5%.

1) Change of V_{cm}: As the common mode voltage changes, the total leakage current value also changes (Fig. 10). This is due to the effects described previously, like the bulk effect of

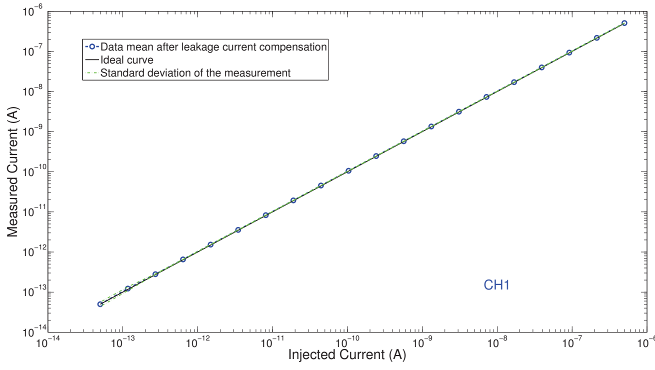

Fig. 13. Injected current versus measured current for CH1 after compensation

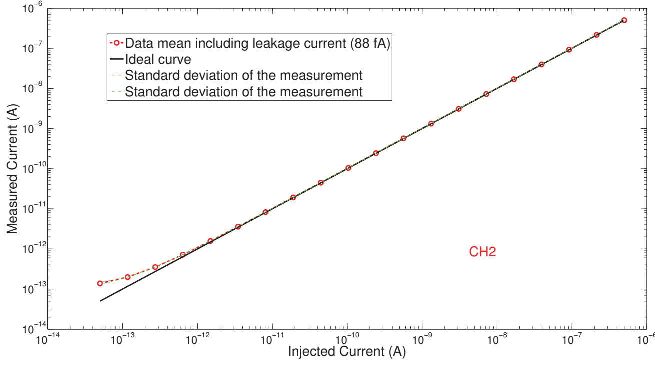

Fig. 14. Injected current versus measured current for CH2

the transistors, the change of the operating conditions of the ESD protection and the leakage of the package because of the different voltages in the adjacent pins. The fact that the total leakage current in a channel with normal ESD protection is affected by a change in the V_{cm} can be used in order to find the V_{cm} value at which there is no net leakage current (that in this case was V_{cm}= 1.58 V). A control circuit could be built in order to eliminate the total leakage current I_{leak}.

2) Leakage current subtraction: The leakage current of CH2 is negative, so it was accurately measured over a long period of time with the CFC. If this constant leakage current value is stored and then subtracted from the current I_{total} that is calculated by observing the number of counts in the measuring time, the input current I_{in} can be measured.

D. Maximum current

The charge injection circuit must recharge itself after a discharge and in the initial control system the discriminator output going low is what triggers the second part of the cycle. In Fig. 15, some noise on the signal in current above 500 nA prevents the integrator output from going below the threshold after a discharge, resulting in discriminator output remaining high. The control system was adapted to work in a level sensitive mode, where as long as the discriminator output remains high, the charge injection circuit alternates between charge-discharge cycles continuously. This is shown in Fig. 16.

By introducing this control circuit, maximum currents up to 5 μA can be measured and the dynamic range is increased as shown in Fig. 17. The system was tested in synchronous

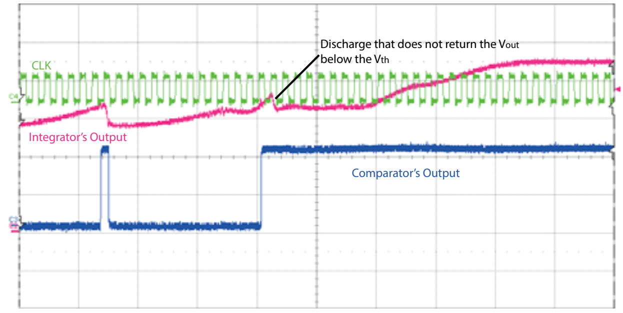

Fig. 15. V_{out}, f_{clk}, V_{Dout} waveforms at the oscilloscope

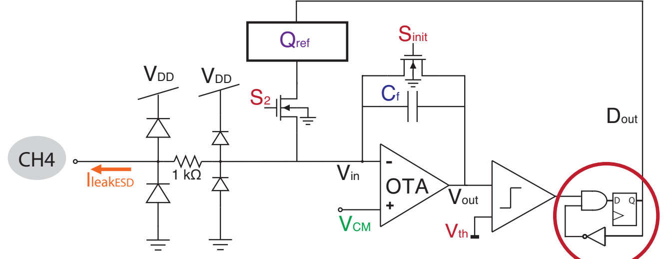

Fig. 16. CH4 with control circuit for dynamic range increase

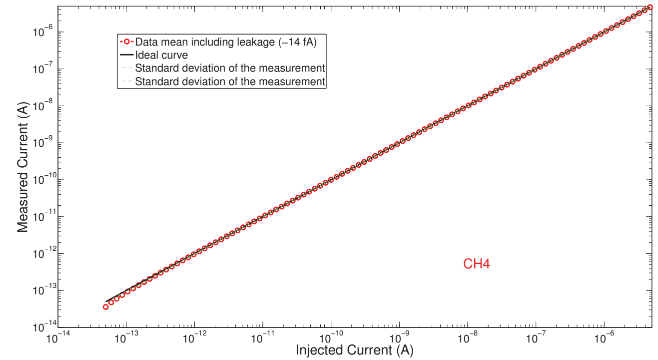

Fig. 17. Injected current versus measured current for CH4

and also asynchronous mode since CH4 had the possibility to bypass the clock and activate the discharging circuit externally. The asynchronous mode operated better compared to the synchronous due to the absence of the clock. Moreover the V_{out} increase after the V_{th} crossing was always constant and did not depend on the phase of the next clock edge. Compared to the asymptotic behavior explained in Eq. 8 that represents the maximum possible error, the duration of the signal that manages the charge injection is critical. With the new control circuit, the number of charge injections increases, the experimental results are better and the error is lower. However, the error does remain dependent on the C_{ref} discharge timing.

V. Conclusions

The methodology of designing and measuring all the different sources of leakage current present at the input of a sub-picoampere current digitiser was presented. The current-to-digital converter is able to measure ultra-low currents comparable to the leakage currents of a CMOS device. The sources of leakage currents were identified, minimised and measured.

Measurement results of currents over 8 decades produced by an accurate current source were presented. A control circuit was also added to increase the performance in the maximum current range. The proposed ASIC can be used as the front-end for ionisation chambers for radiation detection. This chip will be revised and incorporate auto-calibration for long term stability and leakage current compensation.

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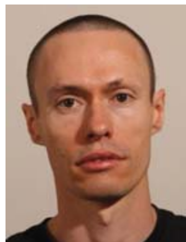
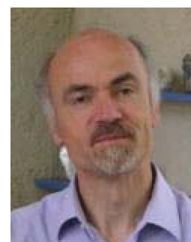


Matthew Noy Dr. M. Noy was born in the UK in 1978 and studied Physics at Imperial College, being awarded M.Sci. and Ph.D. degrees in 2001 and 2004 respectively. Since then he worked in the domains of medical imaging and instrumentation for particle physics. He joined CERN as an electronic engineer in 2009, working mostly on the data acquisition systems for and characterisation of high time precision hybrid pixel detectors.

Francis Anghinolfi received the M.S. degree in electronics from the Institut de Chimie et Physique Industrielle de Lyon (now ECP Lyon) in 1977. He specialized in analogue microelectronics design, working for ST Microelectronics and Motorola Inc. He is since 1988, at CERN, Geneva, Switzerland, developing low-power microelectronics analogue and digital circuits for the High-Energy-Physics experiments. He has contributed to several of the ASICs currently operating with the Large Hadron Collider (LHC) and is now engaged in the development of advanced ASICs for the future particle colliders.

Daniel Perrin was born in 1963 in France. After receiving a diploma in electronics from the University Institute of Technology of St-Etienne in 1983 he worked for CERN as a Electronics Technical Engineer for the development of the control units of the electrostatic separators for the Large Electron-Positron (LEP) collider. In 1992 he joined the CERN Radiation Protection Group for which he designed and developed instrumentation for ionising radiation measurement. Since 2001 he is Head of the Instrumentation and Logistics Section of the CERN Radiation Protection Group. He led projects for the design and the supply of the radiation monitoring system for the Large Hadron Collider (LHC) and the injector chain. Since 2013 he manages the RAdiation Monitoring System for the Environment and Safety (RAMSES) Programme at CERN.



François Krummenacher Born in Lausanne, Switzerland, in 1955, François Krummenacher received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL) in 1979 and 1985 respectively. He has been with the Electronics Laboratory of EPFL since 1979, working in the field of low-power analog and mixed analog/digital CMOS integrated circuit design, as well as in deep sub-micron and high-voltage MOSFET device compact modeling. Dr. Krummenacher is the author or co-author of more than 100 scientific publications in these fields. Since 1989 he has also been working as an independent consultant, providing scientific and technical expertise in IC design to numerous local and international industries and research labs.

Maher Kayal received M.S. and Ph.D degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) in 1983 and 1989 respectively. He has been with the Electronics laboratories of the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) since 1990, where he is currently a professor and director of the ”Energy Management and Sustainability” section. He has published many scientific papers, coauthor of three text books dedicated to mixed-mode CMOS design and he holds 10 patents. His technical contributions have been in the area of analog and mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing and green energy management.