SPICE Simulation of Passive N-type Guard Rings in Smart Power ICs

Pietro Buccella, Camillo Stefanucci, Jean-Michel Sallese, and Maher Kayal

***Abstract*—When designing in Smart Power technologies, TCAD simulations are mandatory to design effective passive protections against parasitic couplings due to minority carriers. The objective of this paper is to propose a SPICE-based approach to characterize electrical key parameters of a passive protection directly within standard IC design flow avoiding time consuming TCAD simulations. Our approach consists in integrating a new substrate model in SPICE to enable designers to derive themselves process specific design rules and reduce substrate couplings. This methodology enables designers to access valuable results in the early stage of IC design, where before such results could be obtained only in the final verification step.**

***Index Terms*—Substrate modeling, noise coupling, power parasitic modeling**

I. Introduction

In most integrated circuits, the parasitic couplings through the substrate may impact the overall functionalities of the circuit. For this reason, special attention must be paid to both design and layout of circuits in order to minimize such couplings on the chip. In low voltage CMOS technology, substrate noise is generated by the switching activity of digital sub-circuits. Unwanted signals are injected into the substrate through the reverse-junction capacitances [1] or by impact ionization due to hot carriers [2]. Methodologies for characterization, modeling and ways to suppress substrate noise have been detailed in the literature [3] [4] [5].

In high voltage technologies (called Smart Power technologies), additional substrate couplings are generated by forward biased parasitic junctions. Applications for the industrial and automotive market often require circuit solutions for driving inductive loads such as solenoids, relays and DC motors [6]. A way to drive such inductive loads is to control the flowing current through a low or high side switch with a freewheeling diode. When the transistor switches off, the inductor load current causes the switch drain voltage to go beyond supply levels and limited by the freewheeling diode clamp.

In order to reduce the number of the application discrete components and thus the Printed Circuit Board (PCB) size, in Smart Power technologies the parasitic body-to-drain diode of a LDMOS replaces the need for an external diode. However, during the switch off state, the freewheeling current flowing in the LDMOS device diode injects current into the chip substrate which couples with the other sub-circuits. This results in the activation of substrate parasitic NPN or PNP bipolar transistors which may significantly impact the operation of the devices on the IC. For example, a latch-up may be triggered by currents collected by any deep n-well used to isolate digital circuits from substrate. Fig. 1 gives an overview of an half-bridge driver with substrate coupling phenomena including substrate current generation and substrate parasitic devices.

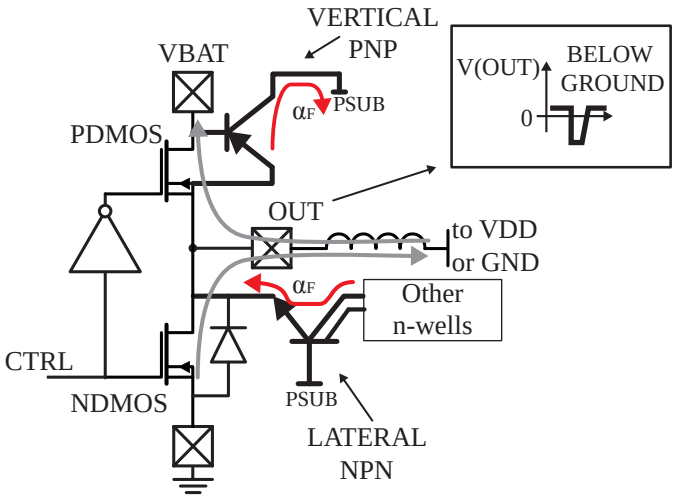

Fig. 1. Half-Bridge inductive load driver configuration with substrate parasitic devices.

Today, these parasitic couplings are often the cause of redesign in Smart Power ICs and they are controlled either through time consuming TCAD device simulations or solved by experienced IC designers [7]. The methods that most effectively reduce such couplings in a chip are based on the physical separation distance and appropriate placement of guard rings that act as protections [8] [9]. Such protections are placed between the emitter and the victims, which are often the sensitive analog circuits. The transport factor α_F, defined as the ratio between the current collected by a victim versus the injected current ($\alpha_F = \frac{I_C}{I_E}$), is the figure of merit commonly used to measure the effectiveness of a protection [10]. The lower/higher the α_F is, the better/worse the protection is. Unfortunately, it is not always easy to estimate the α_F parameter with SPICE simulations. It represents the common-base current gain of the substrate lateral NPN and it is strongly layout and process dependent. Today the α_F is only determined experimentally or through device simulations, as no SPICE-compatible compact model exists for the parasitic substrate multi-collector NPN.

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In this paper a SPICE-based approach to characterize passive protection key electrical parameters such as the α_F is proposed. In section II the design key parameter α_F was simulated with SPICE and compared with TCAD device simulations for a collector placed at different distances from the emitter. Moreover, the effectiveness of a n-well passive protection placed between the injector and the collecting area was demonstrated through the comparison of SPICE simulation results with the measurements of an equivalent test structure. In Section IV the parameter α_F is simulated with SPICE and compared with measurement of a test structure designed in a commercial $0.35\mu m$ Smart Power technology. Moreover, effects due to multiple injectors are discussed.

II. Substrate Currents Protection Strategies

In general, the lateral substrate parasitic NPN gain α_F is an extremely important design parameter when designing Smart Power ICs. Plots showing the ratio of the collected current versus the injected emitter current (α_F factor) as a function of the distance between collector and emitter area d are of interest to the IC designer [11]. Through the α_F factor, these plots provide quantitative information about the optimal distance between sensitive circuitry and the power device to minimize the coupling during steady-state conduction.

In this paper, the major difficulty for deriving a compact model of substrate parasitic BJTs has been overcome by a substrate distributed modeling methodology presented in [12] and [13]. An equivalent substrate schematic is extracted from the layout by mean of diodes, homojunctions and resistances allowing the automatic detection of substrate parasitic BJTs between devices. With this model substrate currents and thus the efficiency of a passive protection can be simulated with SPICE. In this section, the plot of the α_F parameter versus the separation distance d is obtained by SPICE simulation with the substrate model and compared to device simulations. Moreover, the effect of an additional n-well acting as passive protection is simulated with SPICE and compared with TCAD.

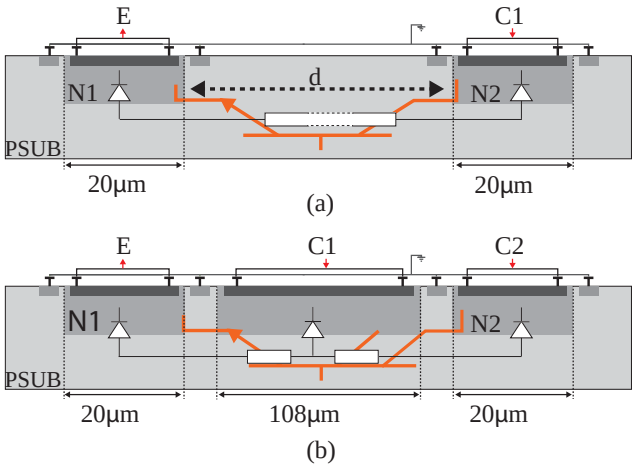

Fig. 2. (a) Two n-well test structure cross section to evaluate the ratio between collected and injected current as a function of the separation distance d. (b) Two n-well test structure cross section placed at a distance of $135\mu m$ with a central n-well acting as passive protection.

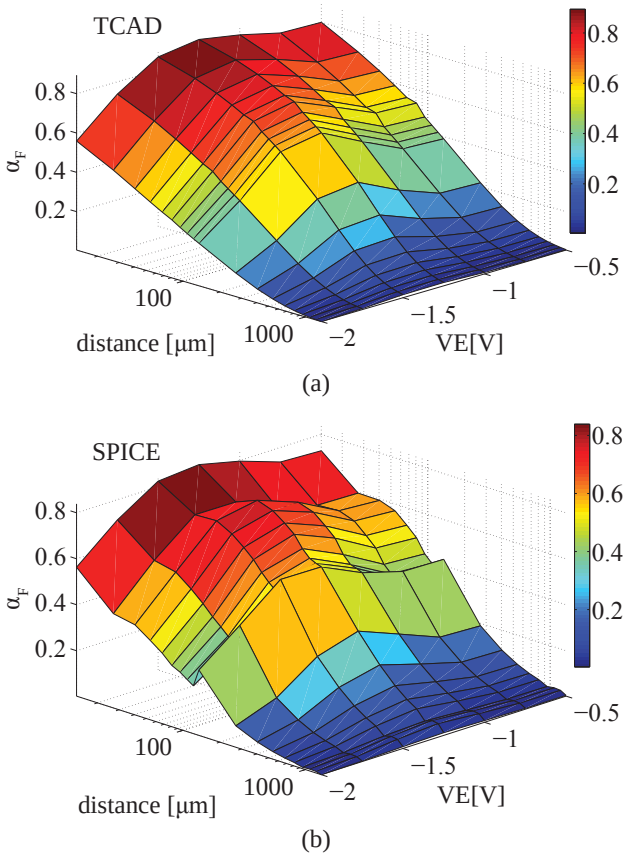

Fig. 3. TCAD (a) and SPICE (b) simulation results of α_F of the substrate lateral NPN transistor as function of distance and of emitter voltage VE.

A. Distance Effect: Two N-wells Coupling Simulation

Today, the α_F parameter value with respect to the separation distance is obtained through the measurement of dedicated test structures including n-wells placed in a single row at various distances d in a p-type substrate [11]. The first n-well represents the emitter region while the second one is the collecting region (left and right side of Fig. 2 (a)). The injection ratio $\alpha_F = I_c \setminus I_e$ is the transport factor of the parasitic lateral substrate NPN transistor. The substrate model is also shown in Fig. 2 (a) as a network of interconnected diodes and resistances.

While SPICE simulations of the substrate model circuit are used to validate the model and determine α_F with respect to distance, TCAD was used to validate the approach with accurate device simulations. For simplicity 2.5 dimensional device simulations of the structure of Fig. 2(a) were done to extract the NPN gain α_F, when having a N-side doping concentration of $Nd = 2 \times 10^{16} cm^{-3}$ and a low doped P-side of $Na = 4 \times 10^{15} cm^{-3}$. To activate the bipolar path in both simulations, the emitter well E was swept from 0 to -2V while the collector well $C1$ was biased at $5V$ thus keeping the substrate voltage at $0V$. Simulations were done with the collector placed at different distances (d) from the emitter E, ranging from $d = 13.5\mu m$ to $d = 1.35mm$. The maximum emitter current is $IE = 200mA$ with $VE = -2V$. Fig. 3 (a) and (b) are a 3D presentation of TCAD and SPICE simulation

results where the coupling parameter α_F is plotted versus the distance and the emitter bias voltage. Despite there being small differences due to the coarse meshing used to derive the SPICE model, there is a good agreement between the circuit model and TCAD from low to high injection levels. In particular, the coupling is maximum at about $VE = 0.8V$ and equal to $\alpha_F = 0.9$, then it decays with the distance $d = 1.35mm$ to $\alpha_F = 0.02$ with most of the injected current flowing toward the substrate contacts (base of the lateral NPN).

B. Passive Protection: Three N-wells Coupling Simulations

To further reduce parasitic couplings, a n-well was placed between the emitter and collector region. The benchmark structure cross section is represented in Fig. 2(b). The central n-well acts as passive protection by providing an additional collector to the parasitic lateral NPN [14]. The distance between the emitter and the sensitive collector C2 is $135\mu m$ and a large central collector ($W_{C1} = 108\mu m$) is inserted between the emitter and the outer collector. The structure was simulated with the SPICE substrate model and TCAD with the same simulation conditions as in previous subsection II-A and results are shown in Fig. 4.

In this case, TCAD and SPICE simulations are also aligned, thus revealing the shielding effect of the protection n-well barrier C1 with respect to the collector C2. The gain α_{F2} is the current gain of the collector C2. The maximum coupling is $\alpha_{F2} = 0.6$ with the collector placed at a distance of $d = 135\mu m$ from the emitter region and with the central collector left floating. The coupling is reduced to $\alpha_{F2} = 0.05(TCAD)$ or $\alpha_{F2} = 0.01(SPICE)$ when the central collector is biased to $5V$. The emitter current is mostly collected by the closer collector C1 ($\alpha_{F1} = 0.8$).

The simulations show the effectiveness of the passive protection C1 with the C2 coupling reduced by a factor of 12. In order to achieve the same amount of coupling reduction in a two well structure with respect to the three well structure of Fig. 2(b), the two wells should be located about $d = 1.35mm$ apart.

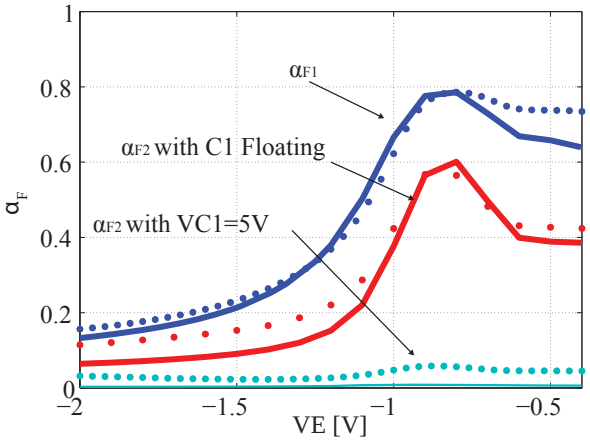

Fig. 4. Simulated α_F of collector C2 with and without C1 acting as barrier. Dots are TCAD simulations while continuous lines are SPICE simulation.

III. Test Structure and Equivalent Substrate Model

A test structure was designed and fabricated with a standard $0.35\mu m$ Smart Power technology to compare measurements with substrate SPICE model simulations. The layout view is shown in Fig. 5 and the cross section is shown in Fig. 6.

The test structure consists of three aligned high voltage n-type wells, each with area of about $15000\mu m^2$. Each well is surrounded by a $4.5\mu m$ wide $p+$ substrate ring connected to the ground. The distances between the n-wells are $80\mu m$ and $75\mu m$, respectively.

The substrate equivalent model of the test structure for SPICE simulation is reported in Fig. 7. The substrate is modeled with a network of lumped devices containing 108 diodes, 4863 resistances and 561 homojunctions. Each device has four terminals and it is descriptive of the well-established drift-diffusion models for the carrier transport in the substrate [13]. The simulation time to compute 201 points in a DC sweep analysis with Spectre was within 5 minutes.

IV. Measurements

With this test structure, different measurements and simulations are performed to reproduce and characterize the behavior of substrate parasitic coupling effects. These include an analysis of distance, the effect of protecting n-rings and the superposition of multiple injectors. For each case, measurements were performed and compared with SPICE simulations. All measurements were done at room temperature with a HP 4142B modular DC source.

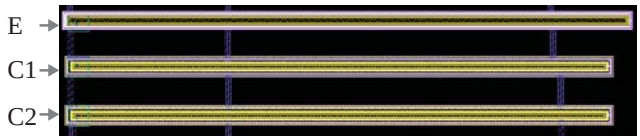

Fig. 5. Test structure layout designed and fabricated with a $0.35\mu m$ high voltage technology

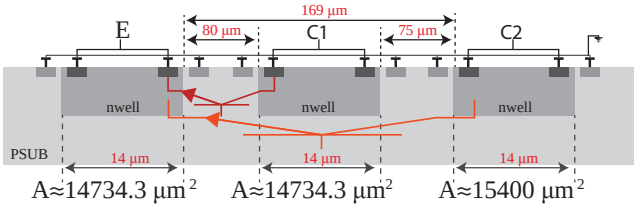

Fig. 6. Test structure cross section: three aligned high voltage n-type wells ($15000\mu m^2 area$). Each well is surrounded by a $4.5\mu m$ wide p+ ring connected to the ground. Two parasitical lateral NPNs were individually activated during measurement and simulation to measure the α_F parameter.

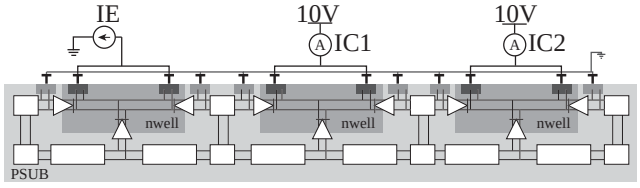

Fig. 7. 2D Test Structure cross section equivalent substrate model for SPICE simulations.

A. Collected Current Dependency Over Distance

The set-up used to measure and simulate the collected current dependency over distance is shown in Fig. 7. A current source is connected to the terminal of the n-well E. A current of up to $120mA$ is drawn from the emitter E while $C1$ and $C2$ are biased to $10V$ one at a time. The whole injected current flows into the substrate and, under these bias conditions, the flow is split between the substrate contacts and either the collector $C1$ or $C2$ (C1 and C2 are biased one at a time in this set-up). Thus, two parasitical lateral NPNs are individually activated with different base widths.

Results for α_F issued from simulation were verified with measurements. Both the simulation and measurements are shown in Fig. 8, confirming how the coupling strongly depends on the spacing between injector E and the collectors ($C1$, $C2$). As expected, this relationship applies to each case, regardless of the level of injected currents.

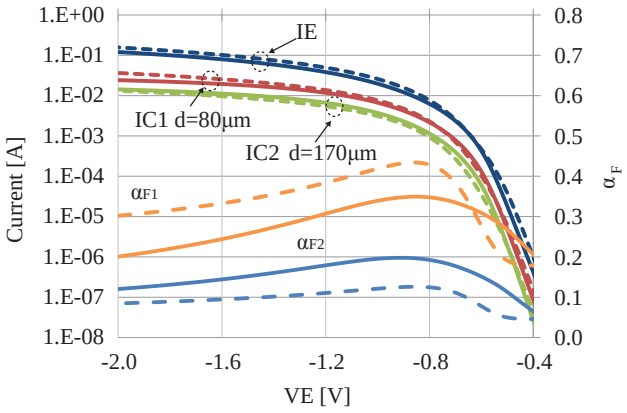

Fig. 8. Simulated and measured substrate lateral NPN current at terminal $C1$ and $C2$ as a function of emitter voltage VE. The common base gains α_{F1} and α_{F2} were measured to either C1 or C2 alone (the other n-well is floating). Dotted lines are measurements while continuous lines are SPICE simulations.

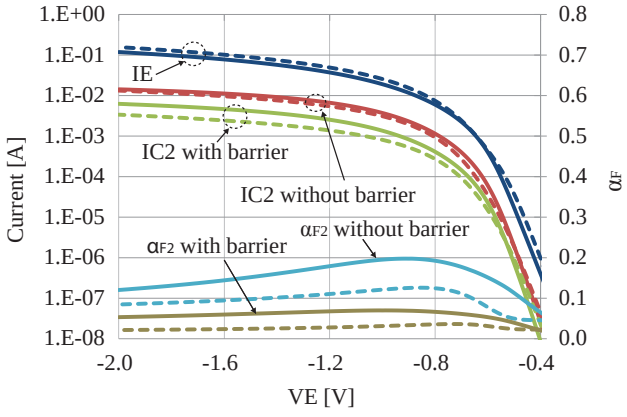

Fig. 9. Simulated and measured α_F of collector C2 with and without C1 acting as barrier. Simulation and measurement are aligned revealing the shielding effect of the protection n-well barrier C1 with respect to the sensible collector C2. Dotted lines are measurements while continuous lines are SPICE simulations.

B. N-well As Passive Protection

In order to show the effect of an n-well protection, the same set-up was simulated and measured to show the shielding effect of $C1$ with respect to the collector $C2$. This case represents the well-known aggressor-victim situation which occur in a chip. To prevent the substrate parasitic current from reaching other sensitive circuits (i.e. $C2$), an additional n-type well is placed between the emitting region E and $C2$. The added n-well $C1$ acts as the preferred collector [15].

A current of up to $120mA$ was drawn from the emitter E while $C2$ was biased to $10V$ and $C1$ left floating. Simulation and measurements were repeated with $C1$ biased to $10V$, activating a double collector lateral NPN transistor. Measurements were confirmed by simulations (see Fig. 9), revealing, as expected, the shielding effect of the n-well protection $C1$ with respect to the sensible collector $C2$. With the introduction of a connected n-ring between the emitter E and the collector $C2$, the current collected by $C2$ is reduced by a factor of four.

C. Double-Injection Situation

When multiple power transistors are integrated in the same IC (i.e. for multi-channels driving applications), several injectors may be activated at the same time. To some extent, the current collected by victims is the cumulative effect of the injected currents [16]. However, the interaction between the injectors changes as a function of their bias voltage with respect to the substrate. A NPN transistor can operate in different modes and consequently it can conduct current in both forward active and reverse active operation modes, depending on the emitter-base and collector-base junctions bias levels. To reproduce these situations, the injection of substrate currents is achieved by simultaneously forward biasing the two substrate junctions $E1$ and $E2$. In the set-up shown in Fig. 10, terminals $E1$ and $E2$ are biased negatively with respect to the substrate with a parametric sweep of voltages $VE1$ and $VE2$ in the range of 0 to $-2V$.

Measurement and simulation results are shown in Fig. 11(a) and (b), where the current through $E2$ is plotted versus $VE1$ and $VE2$. As shown in the graphs, $E2$ current flow changes direction: the current is positive when it enters terminal $E2$, but it becomes negative when it leaves the terminal. This means that $E2$ behaves as an emitter or collector, depending on $E1$ and $E2$ relative emitter biasing conditions with respect to the substrate.

The plots of Fig. 11 show the smooth transition from forward-active to reverse-active conduction mode on the lateral NPN, which is predicted accordingly by the substrate SPICE model.

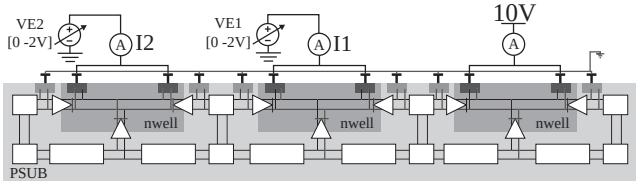

Fig. 10. Set-up for measurement and simulation of injectors effects. The equivalent substrate model for SPICE simulations is also shown.

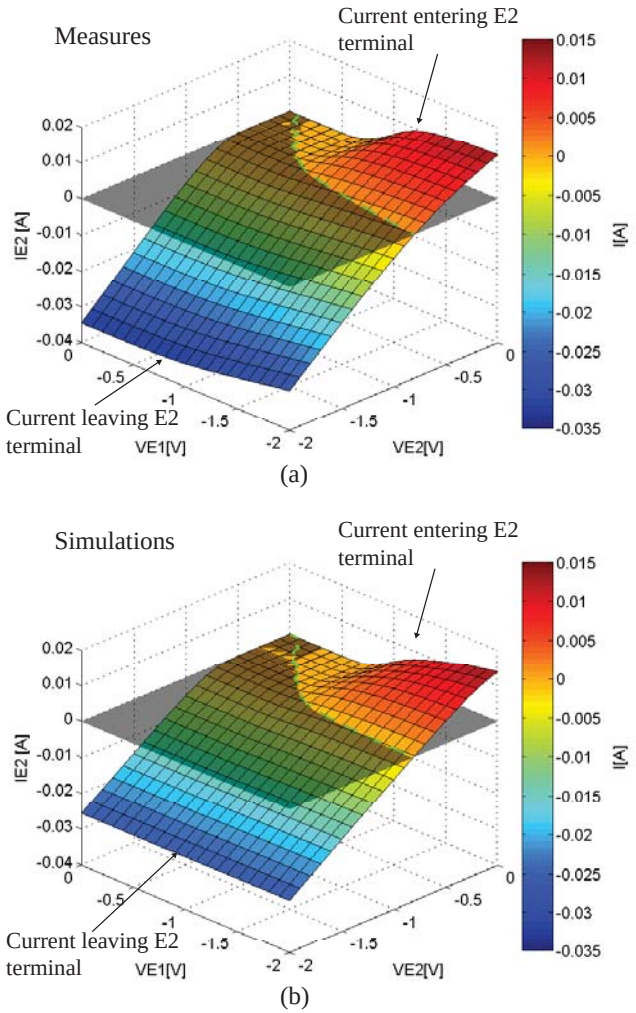

Fig. 11. Measurement and simulation results of $E2$ current in a double emitter situation.

V. Conclusion

In this paper, an equivalent electrical circuit of the substrate has been exploited to simulate with SPICE the efficiency of a n-well acting as passive protection. Simulation of the substrate model and its verification by 2D numerical simulation and by experimental data was reported. This paper provides a SPICE-based approach for the estimation of passive protection effectiveness and clear insight can be derived from the SPICE simulation results. Moreover, this approach precisely predicts substrate currents even in more complex situations with more emitters injecting a substrate current at the same time. This approach opens new horizons to design efficient passive protection and minimize couplings in Smart Power ICs.

Acknowledgment

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