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A Cost-Effective Resonant Switched-Capacitor DC-DC Boost Converter – Experimental Results and Feasibility Model

Research Article

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Abstract: This paper presents the results of experimental research of a resonant switched capacitor voltage multiplier in a cost-effective topology (CESCVM) with a limited number of active switches. In the charging mode of the switched capacitors, the converter utilizes only one active switch and a required number of diodes. Therefore, the cost of the converter is decreased as compared with that of a classical SCVM converter, owing to a lower number of switches and gate driver circuits, as well as a smaller PCB area. Moreover, the CESCVM has simpler control circuits and higher reliability. This paper presents the original experimental results of the operation of the CESCVM converter. A concept of the bootstrap supply of gate drivers of the flying switches is also examined.

Keywords: *DC-DC converter • switched-capacitors • voltage multiplier • charge pump • ZCS*

1. Introduction

Switched-capacitor converters have some important advantages in comparison to other concepts, such as high voltage gain, quasi inductiveless design, low weight, high efficiency and very simple control. Switched-capacitor (SC) DC-DC converters represent a wide family of topologies, with multiple representation in the scientific literature (Alam and Khan, 2014; Ben-Yaakov, 2012; Cao and Peng, 2010; Cervera et al., 2015; Cheung et al., 2013; Evzelman and Ben-Yaakov, 2013; Ioinovici, 2001; Kawa and Stala, 2016; Kawa et al., 2016; Lei and Pilawa-Podgurski, 2015; Mak et al., 1995; Mondzik et al., 2016; Waradzyn et al., 2017a,b) or can be used as a part of complex converters (Ye et al., 2014; Zajac et al., 2017).

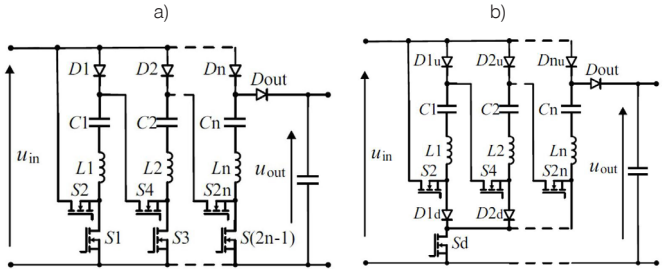

Fig. 1. DC-DC converter in the topology of: (a) basic Resonant Switched-Capacitor Voltage Multiplier (SCVM), (b) Cost-Effective Resonant Switched-Capacitor Voltage Multiplier (CESCVM)(Waradzyn et al., 2017a)

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As typical switch-mode DC-DC boost converters can achieve very high efficiencies and regulation capabilities, the SC-based converters, such as SC multipliers (Kawa et al., 2016; Mondzik et al., 2016; Waradzyn et al., 2017a,b), can be an alternative option for the reason of high voltage gain capability and quasi-inductiveless design. The voltage gain of the SC converters can be achieved by multiplication of the source voltage and can depend on the number of SC cells. The SC-based topologies are also proposed as high voltage pulse generators (Alijani et al., 2016; Redondo, 2010; Sakamoto et al., 2012). Inductiveless design is a significant benefit in the converters where the volume and weight reduction is required, and in systems operating at high temperature (not applicable for ferrite-core chokes).

The basic switched-capacitor voltage multiplier (SCVM) (Fig. 1a) is an interesting and attractive topology from the standpoint of applications, owing to its relatively simple and modular composition. This converter can create a representative research model for the investigations of problems related to SC topologies. High efficiency of the power SC converter is achieved by the application of resonant circuits for charging and discharging of the switched capacitors. However, it contains a large number of active switches, especially in the case of high-voltage-gain units.

Therefore, a concept of cost reduction by using topologies with a lower number of transistors, such as the Cost-Effective SCVM (CESCVM) shown in Figure 1b (Waradzyn et al., 2017a), should be analysed. The topology is well-established, but to find its advantages and disadvantages, the experimental results of a particular design are interesting. This paper presents the results of the analytical and experimental research of the CESCVM, demonstrating the operation and feasibility of the converter. A simplification of the power circuit of an SCVM is demonstrated where some transistors are replaced by diodes. A very simple operation of the gate driver circuits is presented as well, where the bootstrap concept is introduced for all the high-side switches. The CESCVM efficiency is also precisely measured in the experimental setup, to verify the expected problems with power losses.

2. Basic operation of the converters

The SCVM (Fig. 1a) consists of *n* cells, each with a switched capacitor, an inductor and semiconductor devices responsible for charging and discharging of the capacitor. In its basic switching strategy [two-stage (*TS*) switching], the converter operates in two cycles within each switching period T_S (Fig. 2): STAGE I (time interval T_{SI}), when the switched capacitors are being charged from the input source with the switches $S_1, S_3, \ldots, S_{(2n-1)}$ turned on, and STAGE II (time interval T_{SII}), when the switched capacitors are being discharged to the output capacitor with the switches $S_2, S_4, \ldots, S_{2n}$ turned on. Owing to the resonant character of the circuit, the current oscillates, and the converter can operate in the ZCS mode.

If the converter is not overloaded, the voltage ratio of the idealized converter depends only on the number of switching cells (Kawa et al., 2016; Waradzyn et al., 2017a,b)

$$U_{\text{out}} = (n+1)U_{\text{in}}. \tag{1}$$

The basic SCVM can be modified by replacing the transistors $S1, S3, \ldots, S_{(2n-1)}$ with a single transistor S_d and diodes $D1_d, D2_d, \ldots, D_{(n-1)d}$ (Fig. 1b). Owing to this, there is a cost reduction – instead of n transistors with their gate driver circuits, only one transistor and n - 1 additional diodes are used. This converter (CESCVM – Cost-Effective Voltage Multiplier) operates in a similar way as the SCVM (Fig. 2).

3. Current and voltage stresses

Comparison of the SCVM and CESCVM (Fig. 1) shows that the current flowing through transistor S_d in the CESCVM is *n*-fold than that flowing through transistors $S_1, S_3, \ldots, S_{(2n-1)}$ in the SCVM. The currents in the diodes $D_{1d}, D_{2d}, \ldots, D_{(n-1)d}$ equal those in transistors $S_1, S_3, \ldots, S_{(2n-1)}$ in the SCVM. The current stresses of the other power-electronic devices remain the same as in the SCVM.

The voltage stresses on the transistors in the basic SCVM are dealt with in detail by Waradzyn et al. (2017b). In the CESCVM, the voltage across the transistor S_d is the same as that on $S_{(2n-1)}$ (low-side transistor nearest the output) in the SCVM, and equal to nU_{in}. In addition, the sum of the voltages across S_d and D_{1d} in the SESCVM must equal the voltage on S_1 in the SCVM. Hence, the voltage stresses are: U_{in} for S_1 (Waradzyn et al., 2017b) and $-(n-1)U_{in}$ for D_{1d}. In a similar way, from $2U_{in}$ on S_2 (Waradzyn et al., 2017b), we obtain $-(n-2)U_{in}$ on D_{2d}, and so on. Therefore, as far as the low-side diodes in the CESCVM are concerned, the devices placed closer to the input side

are exposed to higher voltage stresses than the more distant ones. This is contrary to the voltage stresses of S_1, S_3, … in the basic SCVM, in which the low-side devices closer to the input experience lower voltages.

The voltage stresses of the power-electronic devices in the CESCVM for $n = 3$ are presented in Table 1. The voltages across transistors S_2, S_4, … equal U_{in} during charging the switched capacitors and can be in the range of $U_{in} \div 2U_{in}$ during the time intervals with zero input current.

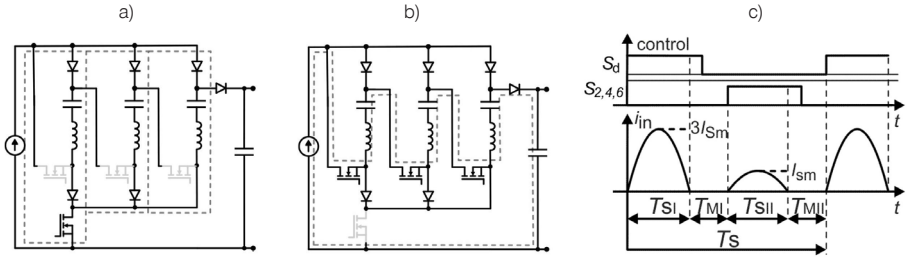

Fig. 2. Operation of CESCVM at $n = 3$: (a) charging and (b) discharging stages, (c) gate control signals and input current waveforms with definition of pulse durations and dead-times for both converters in Figure 1. I_{Sm} – amplitude of current charging the output capacitor

Table 1. Voltage stresses of power-electronic devices in CESCVM (Fig. 1b) for $n = 3$

Device	D_{1u}, $\boldsymbol{D_{2d}}$	D_{2u}, $\boldsymbol{D_{1d}}$	D_{3u}, D_{out}	S_2, S_4, S_6	$\boldsymbol{S_d}$
Voltage stress	$-U_{in}$	$-2U_{in}$	$-3U_{in}$	U_{in} to $2U_{in}$	$3U_{in}$

4. Efficiency of the converters

The efficiency of both converters was analysed in detail by Waradzyn et al. (2017a). According to this reference, the efficiency of the SCVM is as follows:

$$\eta = 1 - \frac{\pi^2 n}{4(n+1)^2} \frac{P_{in} r_S}{U_{in}^2} \cdot \frac{T_S}{T_{SI}} - \frac{\Delta U_{DS}}{U_{in}} - \frac{\Delta W_{sw} f_S}{P_{in}} \tag{2}$$

where n is the number of cells, U_{in} is the input voltage, P_{in} is the input power, $f_S = 1/T_S$ is the switching frequency, $T_{SI} = T_{SII}$ (Fig. 2) is the current pulse duration, r_S is the total resistance of each cell, including MOSFETs resistances, ΔU_{DS} is the voltage drop across each diode, ΔW_{sw} is the energy lost at turn-on in all the MOSFET's resistances in a single switching cycle T_S. It is also assumed that the values of the elements in each cell are the same, both in the circuits of charging and discharging of the cell capacitors, dead-times T_{MI} and T_{MII} (Fig. 2) are the same, and the voltage drops across the diodes remain constant in the conducting state.

In the CESCVM, it is assumed that the resistance of each circuit of charging the cell capacitor, excluding the branch with transistor S_d, is r'_S, the resistance of the branch with transistor S_d is r''_S, the total resistance of each cell in the circuit of discharging the cell k capacitor is r_S, including the resistance of the MOSFET, and ΔU_{DS} is the voltage drop across each diode. Other assumptions are that $\Delta W_{sw}'$ is the energy lost at turn-on in all the MOSFET's resistances in a single switching cycle T_S and the mean and rms values of the currents are the same as in the basic SCVM.

The efficiency of the CESCVM is the following (Waradzyn et al., 2017a):

$$\eta = 1 - \frac{n}{n+1}\left[\frac{\pi^2}{8(n+1)} \frac{P_{in}\left(r_S' + n r_S'' + r_S\right)}{U_{in}^2} \cdot \frac{T_S}{T_{SI}} + 2\frac{\Delta U_{DS}}{U_{in}}\right] - \frac{\Delta W_{sw}' f_S}{P_{in}} \tag{3}$$

The modification of the topology affects the efficiency in two ways. Firstly, instead of conduction power losses in S_1, S_3, …, $S_{(2n-1)}$ in the SCVM, there are conduction power losses in transistor S_d and diodes D_{kd} in the CESCVM. In most cases, the losses in the CESCVM are higher, owing to a higher current through transistor S_d (in regard to that flowing in S_1, S_3, ...) and losses in diodes D_{kd}. Therefore, a transistor with low $r_{DS(on)}$ and diodes of low V_F are required in the CESCVM to minimize these losses. Secondly, switching losses are less in the CESCVM, due to a lower number of transistors. Hence, significant benefits of the application of the cost-effective multipliers are supposed in the systems where switching losses in the transistors represent an important part of total losses (low-power high-frequency systems).

The ratio T_S/T_{SI} can be replaced by $2f_0/f_s$ in (2) and (3), where f_0 is the resonant frequency of the series LC circuit (Table 2) in each switching cell.

Figures 3 and 4 show the ratio of efficiencies of CESCVM to SCVM as a function of switching frequency f_s and power P_{in}, respectively. The parameters of both converters were assumed to be the same, where possible, and correspond to those of the experimental setup presented in Figure 5.

In most cases, the efficiency of the CESCVM is lower than that of the SCVM. The ratio of the efficiencies decreases with decreasing switching frequency f_s and increasing converter power.

The CESCVM can have a similar or even slightly higher efficiency only in the case of operation at low power and high frequency, when the switching losses are significant when compared to the conduction losses.

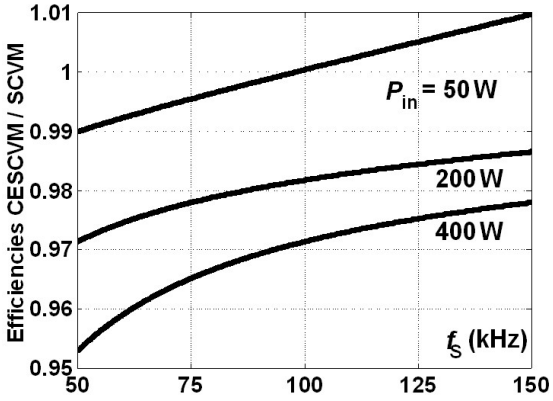

Fig. 3. Ratio of efficiencies of CESCVM to SCVM as a function of f_S for three values of P_{in}: 50 W, 200 W and 400 W. Common parameters: n = 3, U_{in} = 40 V, r_S = 100 mΩ, ΔU_{DS} = 1.1 V. SCVM: ΔW_{sw} = 16 mJ. CESCVM: r'_S = 70 mΩ, r''_S = 50 mΩ, $\Delta W_{sw}'$ = 8 mJ. Calculations based on (2) and (3)

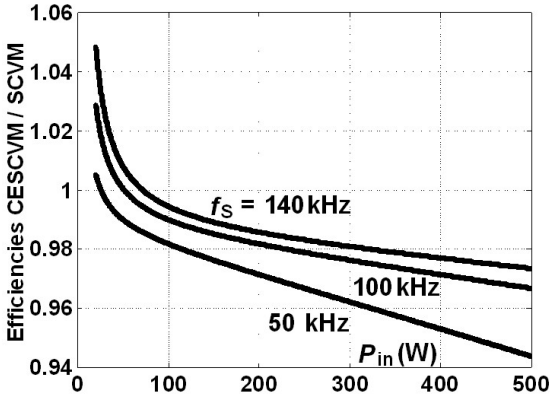

Fig. 4. Ratio of efficiencies of CESCVM to SCVM as a function of P_{in} for three values of f_S: 50 kHz, 100 kHz and 140 kHz. Other parameters as those in Figure 3. Calculations based on (2) and (3)

5. Experimental setup

The experimental tests of the CESCVM were performed on a 3-cell setup with parameters presented in Table 2. The converter was designed using a 4-layer PCB layout with air-based inductances created on the tracks.

The switching frequency of ca. 136 kHz was chosen for the setup operation. It is high enough to properly limit the values and size of the capacitors and inductances, and reasonable with regard to the switching losses and the gate circuit driver performance (Waradzyn et al., 2017a). The achieved inductance of ca. 0.85 μH and the selected capacitance of 1.470 μF in a series connection with the inductance give resonant frequency f_0 of 142.38 kHz.

Zero-current switching is only possible if the switching frequency is equal to or less than the resonant frequency. Therefore, the ZCS operation is possible at the assumed switching frequency. Moreover, the operation near

resonance results in a low value of dead-times, which guarantees high efficiency (Waradzyn et al., 2017a) (the time intervals T_{MI} and T_{MII} are relatively short in comparison to the current pulses duration – Fig. 7).

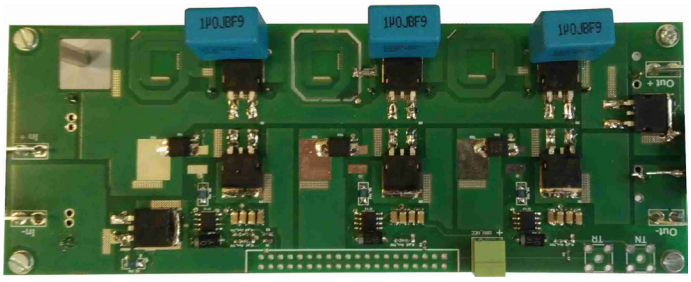

Fig. 5. Three-cell Cost-Effective SCVM

Table 2. Parameters of experimental setup of CESCVM

Items	Specification
Number of switching cells	3
Input voltage	40 V
Low-side MOSFET	IRFS4229PbF
Discharging MOSFETs	3xSIR872
Switched capacitors *Ck*	1.47 µF
Resonant inductances *Lk*	0.85 µH
Diodes	STTH3006

6. Gate driver system

In the CESCVM, the supply system for the gate drivers can still be designed as a bootstrap topology. It resembles that described by Waradzyn et al. (2017a) for the SCVM converter. In the CESCVM, there is a single low-side switch (S_{d}) and n high-side (flying) switches ($S_{2,4,6}$). The bootstrap capacitors of the high-side switches (C_{b}) are charged simultaneously through the low-side transistor and the low-side charging diodes. The supply system for the gate drivers in the CESCVM remains very simple and not expensive. In the experimental setup, IRS2181 gate drivers are used, but only one driver is used for the low-side transistor S_{d} control. The driver system can be further simplified.

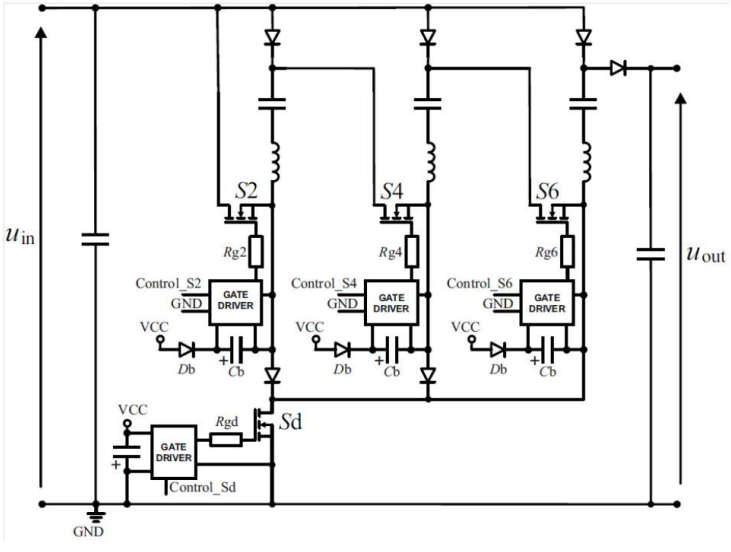

Fig. 6. Proposed gate driver system in CESCVM

7. Experimental results

The operation of the CESCVM is similar to that of the SCVM described by Kawa et al. (2016), Mondzik et al. (2016) and Waradzyn et al. (2017a,b). In the CESCVM, there is only one low-side transistor S_d. Figure 7 presents the experimental waveforms of the control signals for the transistors in the CESCVM, as well as the input current and voltage on a switched capacitor. The results confirm the feasibility of the converter, its operating idea, and the effectiveness of the gate driver system. Due to the impact of parasitic elements, the pulses discharging the switched capacitors are shorter than those that charge these capacitors.

Figure 8 presents the measurements of voltage stresses on the switches. From the results, it follows that the voltage on switch S_d is approximately equal to $3U_{in}$, and the voltage on the series switch S_2 remains on the level of U_{in}.

The waveforms in Figure 9 confirm that the voltage stress on the low-side diode D_{1d}, which is nearer the input, is larger than that on diode D_{2d} (Table 1).

Converter's efficiency η and converter's output voltage U_{out} are presented in Fig. 10, as a function of output power. The highest value of efficiency, equal to 92%, occurs at $P_{out} \approx 100$ W. The efficiency is relatively low in comparison to a typical switch-mode boost converter. It could be improved by using a low-side transistor with low $R_{DS(ON)}$ and diodes of low V_F. Moreover, the comparison can be more beneficial in the case of a high-voltage-gain operation.

The output voltage is lower than the theoretical value of 160 V, and the voltage gain is in the range from 3.91 at 20 W to 3.57 at 260 W.

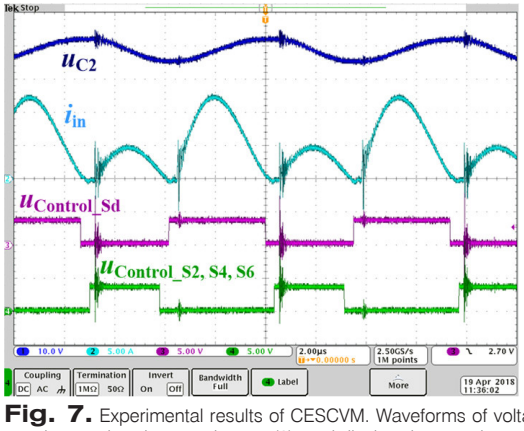

Fig. 7. Experimental results of CESCVM. Waveforms of voltage across switched capacitor C2 (1), input current i_{in} (2) and gate control signals of transistors: charging transistor S_d (3), and discharging transistors S_2, S_4, S_6 (4). $U_{in} = 40$ V, $P_{out} \approx 200$ W, dead-time = 350 ns

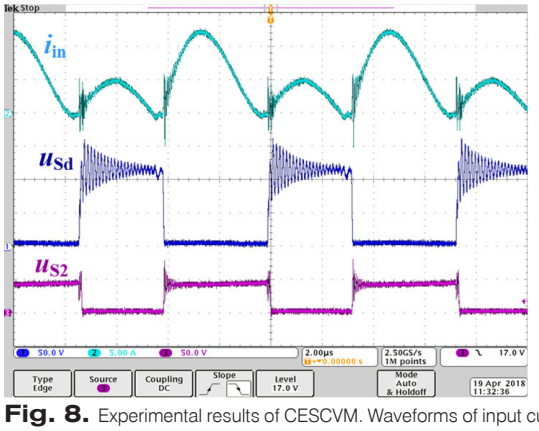

Fig. 8. Experimental results of CESCVM. Waveforms of input current i_{in} (2), voltage across charging transistor S_d (1), and voltage across discharging transistor S_2 (3). $U_{in} = 40$ V, $P_{out} \approx 200$ W

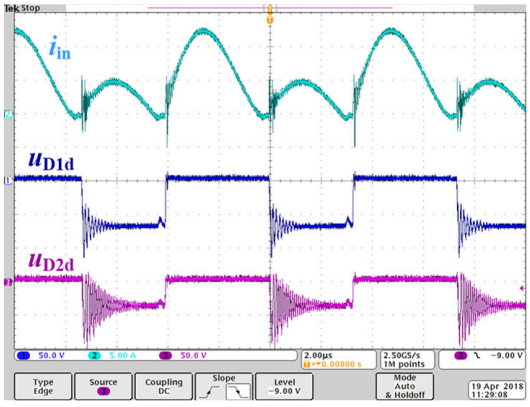

Fig. 9. Experimental results of CESCVM. Waveforms of input current (2), voltage across diode D_{1d} (1) and voltage across diode D_{2d} (3). U_{in} = 40 V, $P_{out} \approx$ 200 W

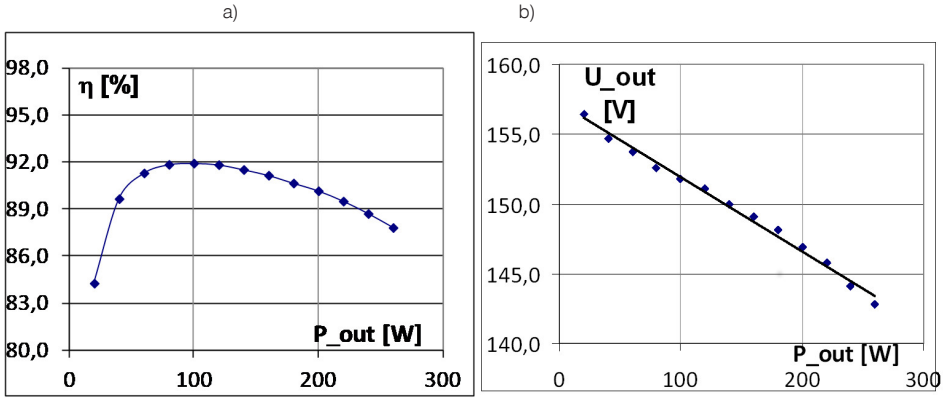

Fig. 10. Experimental results of CESCVM. Converter's efficiency η (a) and converter's output voltage U_{out} (b) vs. P_{out}. U_{in} = 40 V and f_S = 136.6 kHz.

The IR image presented in Fig. 11 confirms that the vast majority of losses is generated in transistor S_d; thus, the efficiency can be further improved by selecting a switch S_d of very low $R_{DS(ON)}$.

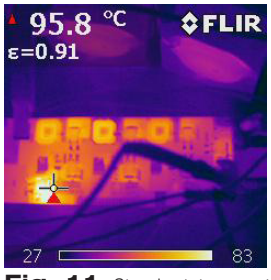

Fig. 11. Steady state operation at 250 W of output power. Hot spot located on transistor S_d.

8. Conclusions

The results of the investigation of a cost-effective switched-capacitor voltage multiplier (CESCVM) make it possible to draw the following conclusions:

- The concept of the CESCVM is feasible,
- The CESCVM was tested in the setup with air-based resonant chokes. This is a significant benefit in comparison to a switch-mode boost converter where a large ferrite choke is used.
- The design with replacing *n* low-side transistors with a single transistor and *n*-1 diodes is not complicated.

This solution reduces the cost of the elements and saves space on the PCB, owing to a lower number of switches and gate driver circuits.

- The CESCVM can operate using a simple and not expensive gate driver system with a supply of high-side switches based on bootstrap circuits.
- The voltage stresses of the additional elements in the CESCVM are not equal. The voltage on the transistor is the same as that on the device nearest to the output in the basic SCVM. The diodes closer to the input side experience higher voltage stresses than those that are more distant. This is contrary to the voltage stresses in a basic SCVM, in which the low-side transistors nearer the input are exposed to lower voltages.
- The analysed CESCVM operates with relatively low efficiency in comparison to a typical switch-mode boost converter. However, the comparison can be more beneficial when high-voltage-gain operation is concerned.
- To improve the efficiency of the SESCVM, a low-side transistor with low $R_{DS(ON)}$ and diodes of low V_F are required. In the analysed setup, a 42 mΩ MOSFET was used.
- The CESCVM can only operate in its basic switching strategy (TS), unlike the SCVM in basic topology.
- In most cases, the efficiency of the CESCVM is lower than that of the SCVM. More significant benefits of the application of the cost-effective multiplier are supposed in the systems where switching losses in the transistors represent an important part of total losses (low-power, high-frequency, high voltage systems).

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