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An improved space vector modulation strategy for common-mode voltage reduction in matrix rectifier

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Abstract: The matrix rectifier modulated by the classical space vector modulation (SVM) strategy generates common-mode voltage (CMV). The high magnitude and high *du/dt* of the CMV causes serious problems such as motor damage, electromagnetic noise and many others. In this paper, an improved SVM strategy is proposed by replacing the zero vectors with suitable couple of active ones that substantially eliminate the CMV. Theoretical analysis proves that the proposed strategy can reduce the amplitude of the CMV to half of the original value. In addition, the quality of the input and output waveforms is not affected by extra active vectors. Simulation and experimental results demonstrate the feasibility and effectiveness of the proposed strategy are shown.

Key words: matrix converter, space vector modulation, common-mode voltage

1. Introduction

The AC-DC matrix converter, or matrix rectifier (MR) [1], is a power conversion topology derived from the well-known three phase AC-AC matrix converter (MC). The MR features several advantages in terms of weight and volume by getting rid of bulky energy storage components, such as the line inductors and the DC-link capacitors in the pulse width modulation (PWM) rectifiers. Besides, the MR can generate DC output voltage with arbitrary polarity and wide-range controllable magnitude while drawing sinusoidal input current from the power source at unity or specified input power factor. These highly attractive characteristics make the MR an ideal future solution for AC-DC power conversion.

Since Donald and Thomas [2] proposed the first modulation technique for MR by utilizing the Venturini switching theory [3], a variety of modulation methods have been published [4]. Among them, space vector modulation (SVM) has been, up to now, a well-known and commonly used modulation method due to its high performance and relative simplicity. However, improperly designed modulation strategy will introduce many problems into the system, including common-mode interference [5], waveform distortion caused by narrow pulses [6], switching losses and so on.

The common-mode voltage (CMV) with high magnitude, high frequency and high variation ratio produced by the power converters can cause early motor winding failure and bearing deterioration, reduce the lifetime of the winding insulation, break the motor insulation easily, and cause wideband electromagnetic interference on the output side. Thus, it is very important to reduce the CMV or limit it within certain bounds for adjustable speed drive systems or other types of load.

The reduction of the CMV in systems fed by MC has been investigated in recent years. Several optimizations and modifications have been proposed in [5, 7-12]. Literature [7] introduced an indirect space vector modulation strategy, which reduced the CMV peak value in MC by 66%, through reassigning the zero switching states. A similar technique can also be found in [8]. A method based on the predictive current control has been proposed in [9]. In order to suppress the magnitude of the CMV in the indirect matrix converter (IMC), the authors of [10] presented a modified double space vector modulation method by selecting the appropriate zero vectors that generate the minimum CMV. Paper [11] went a step further, realized zero-current commutation in the rectify stage of the IMC, meanwhile reduced the CMV to 42%. A new matrix converter based topology to drive a three-phase open-end winding ac machine is described in [12], which can eliminate the instantaneous CMV at the machine terminals. However, all the aforementioned techniques are established for MCs with AC output. The CMV in MR and its suppression strategy has not been studied thoroughly.

The main contribution of this paper presenting a CMV reduction method for MR. In the proposed approach, a group of four non-zero vectors instead of two non-zero vectors and one zero vector used in the traditional SVM strategy are utilized to synthesize the desired output voltage. With replacement of the zero vector by two extra non-zero ones, a 50% reduction of the CMV is achieved. Moreover, the input and output performances of the MR are not deteriorated by the proposed method.

The paper is organized as follows: Section 2 gives a brief review of the MR power circuit and the classical SVM method. Section 3 analyses the CMV of the MR and presents the proposed modulation strategy. Section 4 conducts some simulation and experimental studies, while conclusions are drew in section 5.

2. Matrix rectifier and its modulation strategy

A. Matrix rectifier

By setting the output frequency of the classical nine-switch AC-AC matrix converter to 0, and removing one output leg, several configurations can be obtained [2]. The topology considered in this paper is illustrated in Figure1, where 6 bidirectional switches are employed to connect each output leg to any of the input phases. This type of main circuit topology makes the energy flow of the MR reversible and the polarity of output voltage changeable. Besides, an LC filter is usually required at the input side to improve the source current quality with low harmonic components as well as to reduce the source voltage distortion. The load of the MR is, for simplicity, considered to be inductive.

In Figure1, $i_{a,b,c}$ and $i_{ia,b,c}$ stand for the source currents and the MR input currents, respectively. If the input filter is considered, extra calculations and compensation method resulting from the displacement angle between $i_{a,b,c}$ and $i_{ia,b,c}$ caused by the input filter is needed to achieve a source current in phase with the source voltage [13]. This paper is focused in the development of an improved SVM method to reduce the CMV in MR. Therefore, the input filter is not considered in the analysis.

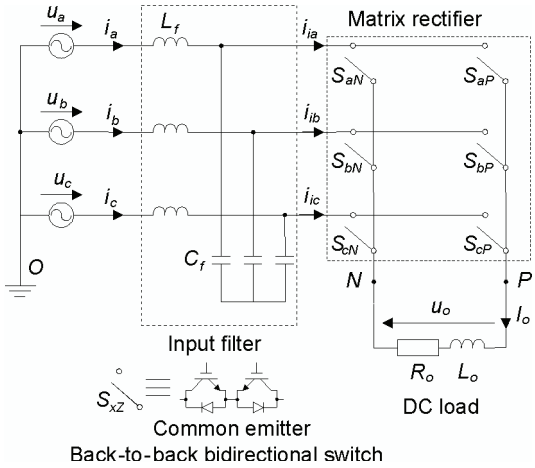

Fig. 1. Matrix rectifier power topology

The bidirectional switches in the MR should be commuted under two basic principles. The first one is only one switch per output leg can be ON to avoid an input line-to-line short circuit, and the second one is one switch per output leg must be ON to avoid open circuit of the inductive load. These restrictions reduce to 9 the feasible switching states as detailed in Table 1. The first 6 switching configurations in group I are called non-zero vectors, determine an input current vector and an output voltage, depending upon the instantaneous output current and the input voltages respectively. The last three in group II, named zero vectors, determine zero input current and output voltage.

Table 1. Switching states and output voltages

Group	**Switching states**	**Conducting switches**	u_o
	$\boldsymbol{I}_1$	S_{aP}, S_{cN}	u_{ac}
	$\boldsymbol{I}_2$	S_{bP}, S_{cN}	u_{bc}
	$\boldsymbol{I}_3$	S_{bP}, S_{aN}	u_{ba}
I	$\boldsymbol{I}_4$	S_{cP}, S_{aN}	u_{ca}
	$\boldsymbol{I}_5$	S_{cP}, S_{bN}	u_{cb}
	$\boldsymbol{I}_6$	S_{aP}, S_{bN}	u_{ab}
	$\boldsymbol{I}_a$	S_{aP}, S_{aN}	0
II	$\boldsymbol{I}_b$	S_{bP}, S_{bN}	0
	$\boldsymbol{I}_c$	S_{cP}, S_{cN}	0

B. Space vector modulation strategy

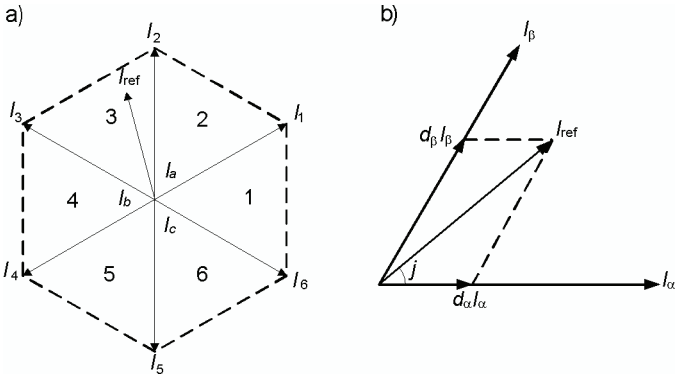

Fig. 2. Space vector diagram and vector synthesis: a) space vector hexagon; b) vector synthesis in one sector

The six non-zero input current vectors in group I divide the space vector hexagon into six separate sectors as illustrated in Figure 2a). In each sector, the conventional SVM method uses two non-zero vectors $\boldsymbol{I}_\alpha$, $\boldsymbol{I}_\beta$ and one zero vector $\boldsymbol{I}_0$ to synthesis the reference input current vector $\boldsymbol{I}_{ref}$ as shown in Figure 2b). In any given sampling instance, the output voltage and the source current displacement angle are known as reference. The phase angle of the source voltages can be recognized by its measurements. Thus, the duty cycles of the vectors $\boldsymbol{I}_\alpha$, $\boldsymbol{I}_\beta$ and $\boldsymbol{I}_0$ are calculated such as in the following [14]:

$$d_\alpha = T_\alpha / T_s = m\sin(60° - \varphi), \tag{1}$$

$$d_\beta = T_\beta / T_s = m\sin\varphi, \tag{2}$$

$$d_0 = T_0 / T_s = 1 - d_\alpha - d_\beta, \tag{3}$$

where m is the modulation index, $m \in [0, 1]$; T_α, T_β and T_0 are the duration times of the vectors $\boldsymbol{I}_\alpha$, $\boldsymbol{I}_\beta$ and $\boldsymbol{I}_0$ in one sampling period T_s respectively; φ is the sector angle and can be obtained using:

$$\varphi = f_{\text{mod}}(\omega_i t - \upsilon, 60°), \tag{4}$$

where ω_i is the angular frequency of the power source; υ is the demanded displacement angle of the source currents; $f_{\text{mod}}(x, y)$ stands for the reminder of x when divided by y.

The three-phase power source is given as:

$$\begin{cases} u_a = U_s \sin(\omega_i t) \\ u_b = U_s \sin(\omega_i t - 120°) \\ u_b = U_s \sin(\omega_i t + 120°) \end{cases}, \tag{5}$$

where U_s is the amplitude of the input phase voltage. Thus, the average values of the output voltage and the source currents in one sampling period are calculated using the source voltages defined in (5) and the duty cycles given in (1)-(3), which result in (6) and (7), after some algebraic calculations:

$$\overline{u}_o = 1.5mU_s \cos\upsilon, \tag{6}$$

$$\begin{bmatrix} \overline{i}_a \\ \overline{i}_b \\ \overline{i}_c \end{bmatrix} = mI_o \begin{bmatrix} \sin(\omega_i t - \upsilon) \\ \sin(\omega_i t - \upsilon - 120°) \\ \sin(\omega_i t - \upsilon + 120°) \end{bmatrix}, \tag{7}$$

From (6) and (7), the MR can output DC voltage with its magnitude continuously changeable from 0 to $1.5U_s$, while drawing sinusoidal currents from the power source with its displacement angle fully controllable by adjusting the parameter υ [15].

Figure 3 shows the switching pattern in one sampling period based on an example that the source voltages are located in Sector 1, the input power factor is unity and the polarity of the output voltage is positive. In this example, the upper switch of the input phase a (S_{aP}) is always ON, while the lower switches S_{aN}, S_{bN} and S_{cN} are modulated according to their corresponding duration times.

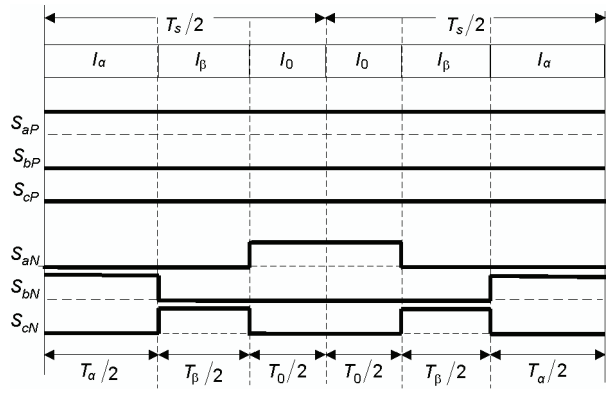

Fig. 3. Switching pattern of the classical SVM in sector 1

3. Proposed PWM method to reduce CMV in MR

A. The CMV of MR

No matter matrix converter with AC output or matrix rectifier with DC output, two types of output voltage are generated while working. One is the differential-mode voltage (DMV), which is available for load; the other one is the CMV, which is defined with reference to the system neutral point and detrimental for electrical equipments. The value of the CMV can be obtained by dividing the sum of the output phase voltages with the number of the output phases. Hence, in the MR system, we have:

$$u_{CMV} = (u_{PO} + u_{NO})/2. \tag{8}$$

Regardless of the influence of the AC source, the CMV is determined by the output voltages which depend only on the switching states of MR. As mentioned in the previous section, assuming the input voltages are lied in Sector 1 and the source current displacement angle is zero. According to (8) and Figure 2, the CMV peak values of all nine feasible switching configurations within this sector are summarized in Table 2.

Table 2. The CMV peak value of switching states within Sector 1

Switching states (output voltage)	**Peak value of u_{CMV}**
$\boldsymbol{I}_1 (u_{ac})$, $\boldsymbol{I}_6 (u_{ab})$	$\sqrt{3}U_s / 4$
$\boldsymbol{I}_2 (u_{bc})$, $\boldsymbol{I}_5 (u_{cb})$	$-U_s / 2$
$\boldsymbol{I}_3 (u_{ba})$, $\boldsymbol{I}_4 (u_{ca})$	$-\sqrt{3}U_s / 4$
$\boldsymbol{I}_a$	U_s
$\boldsymbol{I}_b$, $\boldsymbol{I}_c$	$-\sqrt{3}U_s / 2$

B. Proposed SVM method

The non-zero vectors employed by the conventional SVM method in sector 1 are $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ for a positive output voltage, while $\boldsymbol{I}_3$ and $\boldsymbol{I}_4$ for a negative output voltage. The zero vector utilized is $\boldsymbol{I}_a$. According to Table 2, the maximum CVM equals to the magnitude of the input phase voltage U_s when the zero vector $\boldsymbol{I}_a$ is selected. The same conclusion can be drawn in the other sectors. This state occurs because the zero vector is always selected from the criteria that the number of the commutation times is minimized, subsequently the CMV traces along the envelope of the input phase voltages with the maximum value.

Therefore, In order to suppress the CMV peak value, the switching patterns of the MR should not invoke any zero vector. Still take sector 1 for example. The non-zero vectors $\boldsymbol{I}_2$ and $\boldsymbol{I}_5$, which are not used in the conventional SVM method, produce the output voltages with the same absolute instantaneous value and the opposite polarities. By replacing the zero vector with these two extra non-zero ones, the optimized SVM method can be developed. The duty cycles for each vector are calculated according to the following expressions:

$$d_\alpha = T_\alpha / T_s = m \sin(60° - \varphi), \tag{9}$$

$$d_\beta = T_\beta / T_s = m \sin \varphi, \tag{10}$$

$$d_{01} = d_{02} = T_{01} / T_s = T_{02} / T_s = \frac{1}{2}(1 - d_\alpha - d_\beta), \tag{11}$$

where d_{01} and d_{02} are the duty cycles for the extra non-zero vectors, which are $\boldsymbol{I}_2$ and $\boldsymbol{I}_5$ in this example. One can obtain the mean value of the output voltage and the source currents in one sampling period as indicated by:

$$\overline{u}_o = d_\alpha u_{ab} + d_\beta u_{ac} + \frac{d_{01}}{2} u_{bc} + \frac{d_{02}}{2} u_{cb} = 1.5\ \mathrm{m} U_s \cos\upsilon, \tag{12}$$

$$\begin{bmatrix} \overline{i}_a \\ \overline{i}_b \\ \overline{i}_c \end{bmatrix} = I_o \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha + \dfrac{d_{01}}{2} - \dfrac{d_{02}}{2} \\ -d_\beta + \dfrac{d_{02}}{2} - \dfrac{d_{01}}{2} \end{bmatrix} = m I_o \begin{bmatrix} \sin(\omega_i t - \upsilon) \\ \sin(\omega_i t - \upsilon - 120°) \\ \sin(\omega_i t - \upsilon + 120°) \end{bmatrix}. \tag{13}$$

Form (12) and (13), the DC component in the output voltage and the fundamental component in the source currents are not affected by the modified SVM method, in other words, equals to the values in the conventional SVM strategy given in (6) and (7).

As the conventional SVM strategy, a double-sided symmetrical switching pattern is used. The switching states of the proposed SVM method within Sector 1 are shown in Figure 4 as an example. By utilizing a group of four non-zero vectors listed in Table 3 in six separated sectors, the magnitude of CMV is successfully limited to $0.5U_s$, which is half of the original value.

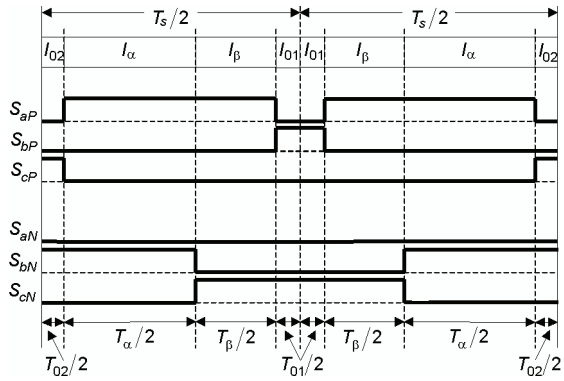

Fig. 4. Switching states of the proposed SVM in Sector 1

Table 3. Sector and switching states of proposed SVM strategy for positive output voltage

Sector	$I_\alpha(d_\alpha)$	$I_\beta(d_\beta)$	$I_{01}(d_{01})$	$I_{02}(d_{02})$	Peak value of u_{CMV}
1	I_6	I_1	I_2	I_5	$-U_s/2$
2	I_1	I_2	I_3	I_6	$U_s/2$
3	I_2	I_3	I_4	I_1	$-U_s/2$
4	I_3	I_4	I_5	I_2	$U_s/2$
5	I_4	I_5	I_6	I_3	$-U_s/2$
6	I_5	I_6	I_1	I_4	$U_s/2$

4. Simulation and experimental results

The parameters for the simulation and the experiment verification are listed down as: the phase voltage of the power supply is 60 V/50 Hz; the DC load has R_o = 25 Ω and L_o = 50 mH;

the input filter parameters are L_f = 3 mH and C_f = 13 μF; the sampling frequency is 6 kHz. These values were not optimized, but rather chosen from those available in the laboratory. The modulation index m is 0.8 in both simulation and experimental research.

A. Simulation results

The MR and the proposed algorithm were then preliminary verified by MATLAB/Simulink software. The simulation results obtained are shown in Figures 5-8, with all switches considered as ideal switch for simplicity.

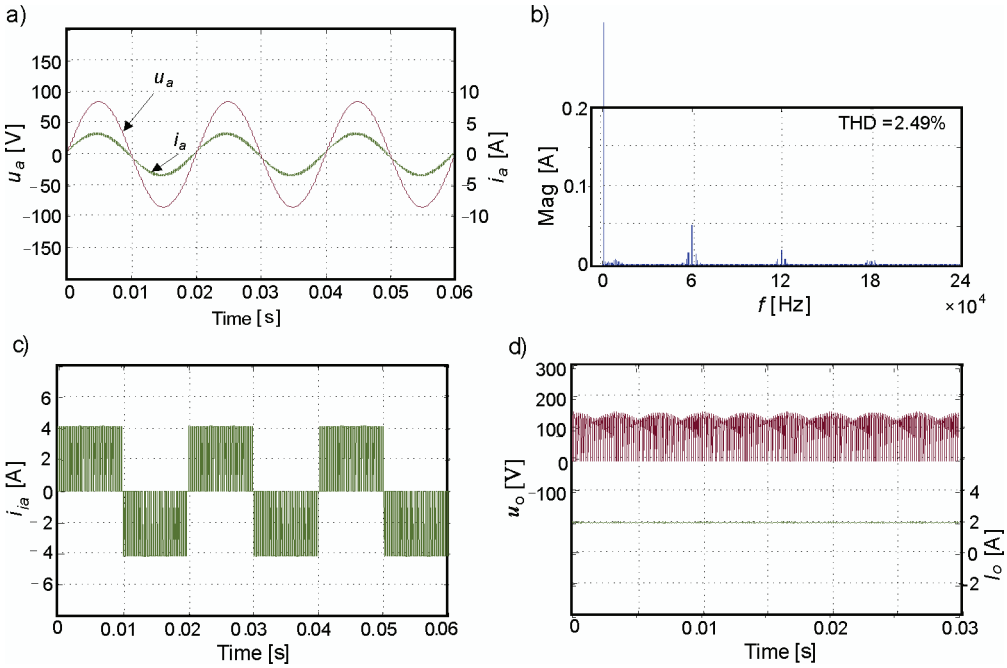

Fig. 5. Simulation results of input and output waveforms with the classical SVM method: a) source voltage and current; b) FFT for source current; c) matrix converter input current; d) output voltage and current

The Figure 5 and Figure 6 show the simulation results for the traditional and the proposed SVM methods, respectively. The figures show waveforms for the source voltage, the source current and its FFT, MR input current, output voltage and current. The CMV waveforms and its FFT for both SVM methods are shown in Figure 7 and Figure 8. Findings verified are summarized as follows:

1) The MR input currents shown in Figure 5c) and Figure 6c) are in phase with the source voltage. Meanwhile, sinusoidal source currents are drawn from the power source by both modulation strategies. However, it should be pointed out that the small phase lead of the source currents observed in Figure 5a) and Figure 6a) is contributed by the input filter, especially the filter capacitor [15], not results from the modulation strategies.

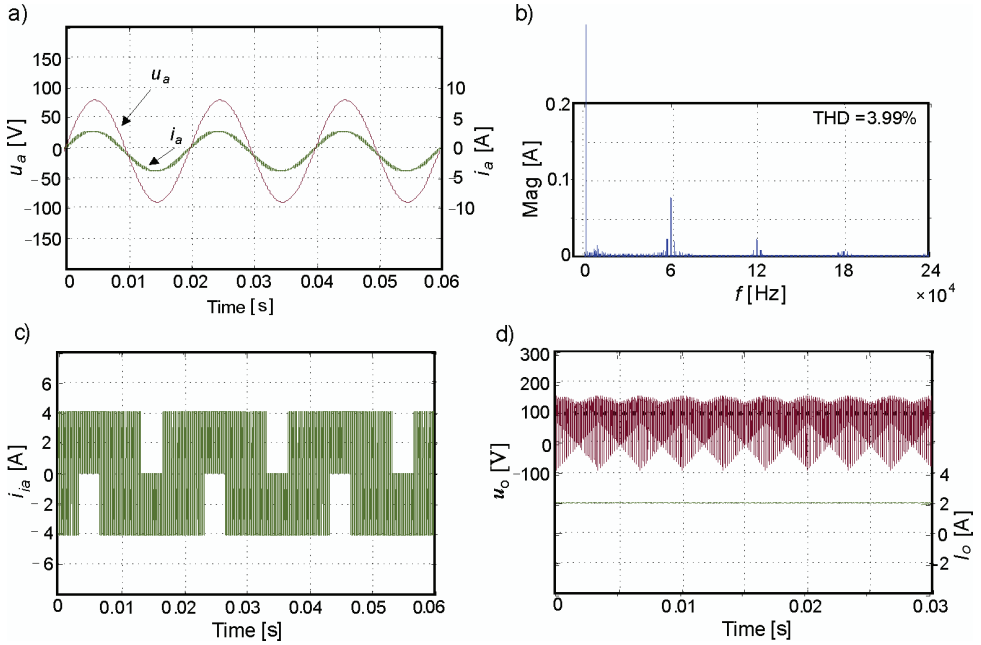

Fig. 6. Simulation results of input and output waveforms with the proposed SVM method: a) source voltage and current; b) FFT for source current; c) matrix converter input current; d) output voltage and current

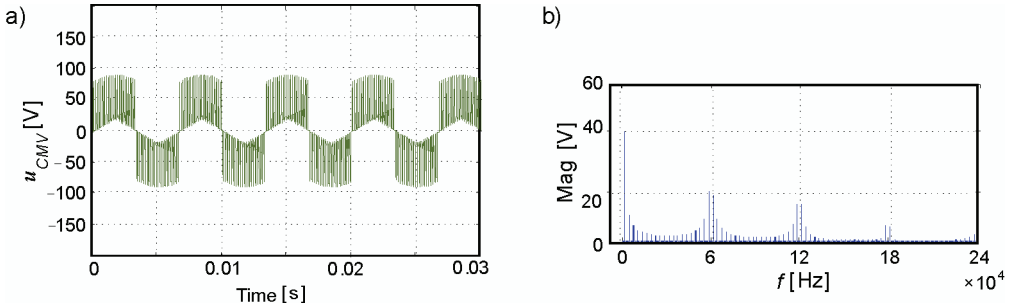

Fig. 7. Simulation results of the CMV and its FFT with the classical SVM method: a) CMV waveform; b) FFT for CMV

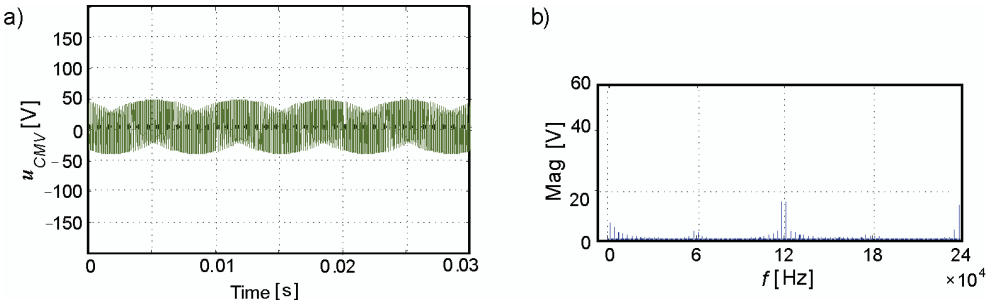

Fig. 8. Simulation results of the CMV and its FFT with the proposed SVM method: a) CMV waveform; b) FFT for CMV

2) Overall, the quality of the input and output waveforms of the MR are not deteriorated by the proposed method. However, this method is not able to neglect the drawback of consisting in the higher total harmonic distortion (THD) of the source current as shown in Figure 6 b) when compared to the current waveform shown in Figure 5b).
3) As shown in Figure 7a) and Figure 8a), the peak value of the CMV in the classical and the proposed SVM methods are 84.5 V and 42.4 V respectively, which means that the proposed SVM method retained the CMV peak value with a 50% reduction. In addition, the FFT analysis shows the harmonic components in the CMV waveform are reduced by the proposed method as well.

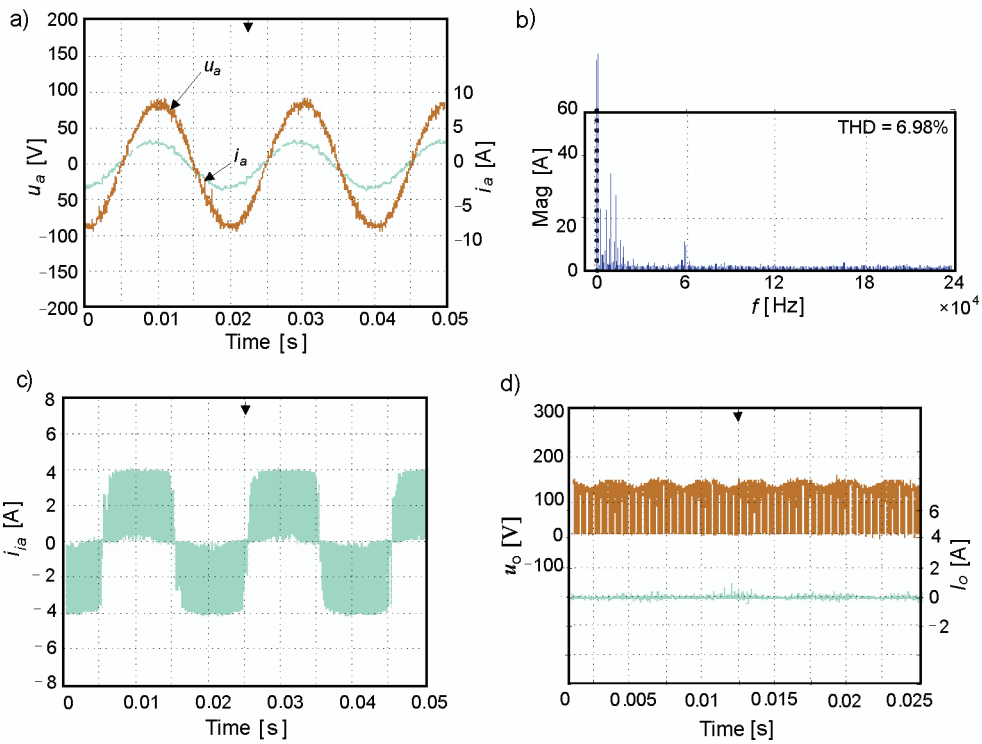

Fig. 9. Experimental results of input and output waveforms with the classical SVM method: a) source voltage and current; b) FFT for source current; c) matrix converter input current; d) output voltage and current

B. Experimental results

For hardware verification, an experimental prototype was designed and built. The implementation setup consists of the control broad containing a digital signal processor (DSP) and a complex programmable logic device (CPLD); an analog broad containing the voltage and the current sensors; power circuit realized by the insulated gate bipolar transistors (IGBT). The DSP, whose model is TMS320F2812 from Texas Instruments, was used for carrying out

the modulation strategies. After that, the duty cycles obtained were transmitted to the XC9572XL CPLD from Xilinx for pulse distribution and current-direction based 4-step commutation.

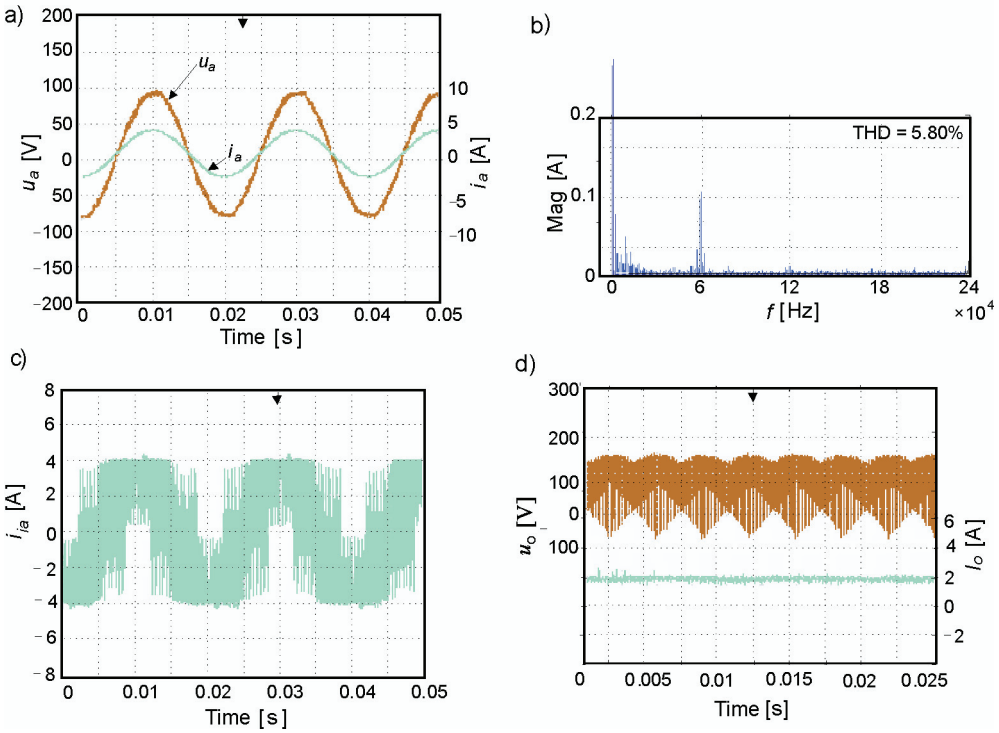

Fig. 10. Experimental results of input and output waveforms with the proposed SVM method: (a) source voltage and current; (b) FFT for source current; (c) matrix converter input current; (d) output voltage and current

In practical applications, the 4-step commutation strategy needs a definite commutation time T_c to commutate the load current from one bidirectional switch to another [16-18]. This requires that the length of every single drive pulse has to be longer than T_c, or detrimental commutation failure will occur [18]. For this reason, the narrow pulses, whose time length cannot fulfill the above-mentioned requirement, are lengthened to T_c in this paper.

The experimental results of the input, output and the CMV waveforms are given in Figures 9-12.

The experimental results of the input and output waveforms obtained are given in Figures 9 and 10, from which the similar findings as listed earlier can be observed, except for two points which have to be noted. First, the THD values of the grid current for the classical and the proposed methods are 6.98% and 5.8% respectively, which are higher than those obtained in the simulations because of the harmonic distortions transmitted from the grid in our laboratory.

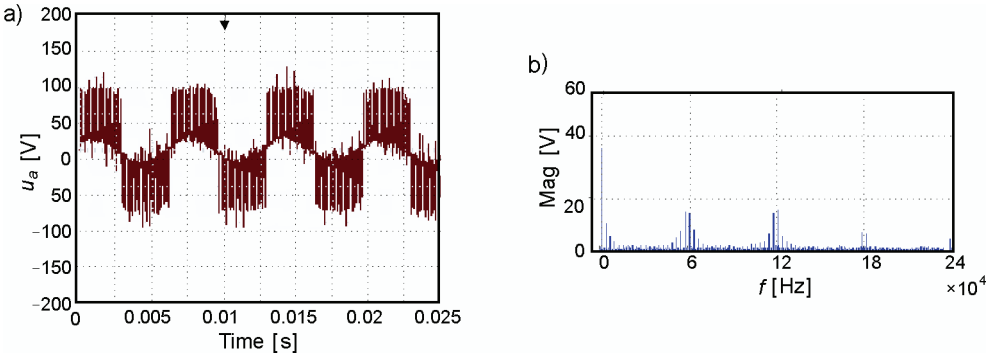

Fig. 11. Experimental results of the CMV and its FFT with the classical SVM method: a) CMV waveform; b) FFT for CMV

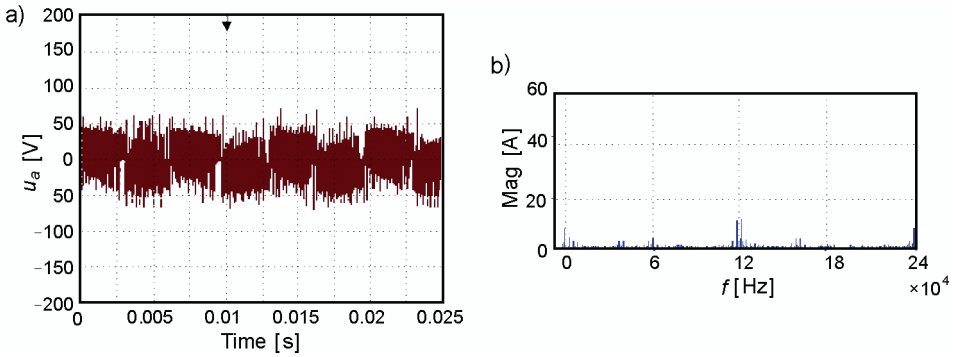

Fig. 12. Experimental results of the CMV and its FFT with the proposed SVM method: a) CMV waveform; b) FFT for CMV

Second, the proposed SVM method shows a better harmonic mitigation with lower THD value of the grid current than the classical SVM method in experiments, which is contrary to the conclusion drawn from the simulation results. The reasons that caused this difference are briefly discussed here. As mentioned before, all narrow pulses are lengthened to the commutation time to avoid commutation failure. But, besides of guaranteeing the safe operation of the real system, the extended narrow pulses cause harmonic distortions in the grid currents. According to Figure 4, the switching pattern employed by the proposed SVM method increases the interval time of the switching between bidirectional switches with lesser narrow pulses produced. Thus, lesser harmonics are introduced into the grid current compared to the classical SVM method.

Figures 11-12 show the CMV waveforms along with their FFT for the classical and the proposed methods, respectively. According to the experimental results, the peak value of the CMV decreased from approximately 83 V generated by the classical method in Figure 11a) to about 42 V generated by the proposed method in Figure 12a). From the FFT results of the CMV, the proposed method shows reduced harmonic components as compared to the classical method. It is clear that the experimental results and the simulation results are totally marched.

5. Conclusion

In this paper, the relationship between the CMV and the switching states has been clarified and an optimized SVM method has been developed to reduce the CMV in MR. By utilizing a group of four active vectors instead of two active vectors and one zero vector to generate the reference output voltage, the proposed method has decreased the peak value of the CMV to 50% of the original value without deteriorating the input and output current control performances of the MR. Simulation and experimental results have validated these advantages, which would strengthen the attractiveness of the MR for industry applications.

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