INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2021, VOL. 67, NO. 1, PP. 49-57
Manuscript received November 7, 2020; revised January, 2021. DOI: 10.24425/ijet.2021.135943

Linearized 9-Bit Hybrid LBDD PWM Modulator for Digital Class-BD Amplifier

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***Abstract*—The paper presents an original architecture and implementation of 9-bit Linearized Pulse Width Modulator (LPWM) for Class-BD amplifier, based on the hybrid method using STM32 microcontroller and Programmable Tapped Delay Line (PTDL). The analog input signals are converted into 12-bit PCM signals, then are directly transformed into 32-bit LBDD DPWM data of the pulse-edge locations within n-th period of the switching frequency, next requantized to the 9-bit digital outputs, and finally converted into the two physical trains of 1-bit PWM signals, to control the output stage of the Class-BD audio amplifier. The hybrid 9-bit quantizer converts 6 MSB bits using counter method, based on the peripherals of STM32 microcontroller, while the remaining 3 LSB bits - using a method based on the PTDL. In the paper extensive verification of algorithm and circuit operation as well as simulation in MATLAB and experimental results of the proposed 9-bit hybrid LBDD DPWM circuit have been performed. It allows to attain SNR of 80 dB and THD about 0,3% within the audio baseband.**

***Keywords*—Class-BD digital audio amplifier, Linearized Pulse Width Modulation (LPWM), Linearized Class-BD Double sided modulation (LBDD), Digital to Time Converter (DTC)**

I. Introduction

CLASS-D amplifier has become a very popular solution for audio applications due to its high efficiency. In this amplifier a pulse code modulation (PCM) data stream is converted to a two level signal (pulse width modulation - PWM), which drives the power MOSFET switches of the output H-Bridge. Output waveform is converted into an analog signal by a low pass filter. The switching elements allow high efficiency, what leads to smaller heat sink and size.

The analog audio Class-D amplifiers convert the input signals in the analogue domain, using most often natural sampled, Class-BD Double sided (NBDD) modulation, which is equivalent to three-level version of Phase Shifted Carrier Pulse Width Modulation (PSCPWM) [1, 2, 3].

In terms of distortion of the modulated PWM signal on the Differential Mode (DM) output of the H-bridge, NBDD modulation is superior, and has by far the most attractive spectral characteristics for all the other PWM methods, because the NBDD frequency spectrum has no harmonics of the switching frequency, and no intermodulation (IM) components around odd multiples of the switching frequency. Practically, effective sampling frequency for DM voltage at the H-bridge outputs is doubled, without increasing the transition frequency on the output [2, 3].

The digital Class-D amplifier (Fig.1b) employs a digital modulator to convert directly N-bit digital pulse-code modulation (PCM) signal input into a train of 1-bit modulated pulses. Two basic modulation techniques may be used: standard Digital Pulse Width Modulation (DPWM), implemented in the form of Uniform sampled modulation (UPWM), or multi-bit Sigma-Delta Modulation (SDM) [4-7], what is presented in Fig.1c and Fig.1d respectively. Class-D concept in such audio system provides an opportunity to remain the audio signal in the digital domain through the amplification process, and conversion to the analogue domain only at the output stage [8].

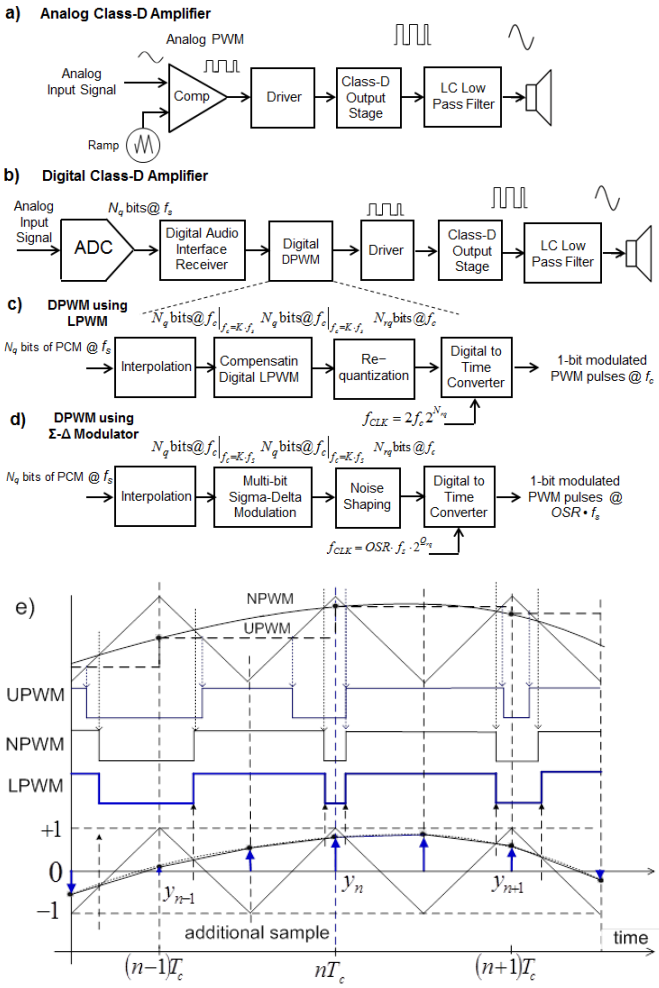

Fig. 1. Comparison of an analog Class-D amplifier (a) with a digital one (b) employing, either DPWM using LPWM algorithm (c) or SDM (d); Comparison of Double sided PWM: NPWM, UPWM, and LPWM (e).

The UPWM process is very simply, unfortunately its fundamental problem is inherent nonlinearity. This nonlinearity may be reduced through increasing the sampling

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rate of the digital input signal (Interpolation), and application of precompensation linearization algorithms. [9, 10].

The precompensation PCM-UPWM algorithms attempt to emulate analog NPWM best possible, using enhanced sampling methods as Pseudo Natural PWM (PNPWM) or Linearized PWM (LPWM) [11-14]. It is possible to realize significant improvements in linearity with the simple LPWM algorithm, such that modulator linearity is no longer an obstacle in DPWM systems. This applies in particular to LBDD PWM, which is equivalent to NBDD PWM with straight line approximated segments of analog modulating signals, which requires higher computational power.

The digital value of the pulse width, calculated with a high resolution of N_q-bit, is then requantized to a lower resolution of N_{rq}-bit output ($N_{rq} < N_q$), to make it possible practical implementation of the digital to time converter (DTC), converting the calculated digital LBDD output data into the physical pulses to drive the H-bridge power MOSFET switches. Practically, even for N_{rq}-bit requantized resolution of the digital output, a required modulator clock frequency f_{CLK} is too high to implement the DCT, therefore to circumvent the excessive clock speed problem, most often a hybrid DCT is used [12-15], which integrates the counter method and a method using the programmable tapped delay line (PTDL).

Digital small power Class-D amplifiers most often use modulator based on a multi-bit SDM (Fig.1d), with a similar topology as that one employing LPWM [4-7, 11]. The algorithmic transformation of the digital PCM signal to PWM signal is moved into the closed SDM loop, thus the noise and distortion generated during the transformation are suppressed by the high gain of the forward loop of the SDM. The interpolation factor allows a trade-off between modulator linearity, dynamic range and factors relating to the power conversion as efficiency and power stage linearity.

The SDM is a more linear method, if the presence of idle tones is reduced by dithering. However, SDM produces bit-stream which is uniformly distributed over the oversampling period, causing high switching frequencies in the output power stage. Compared to LPWM, SDM needs a much higher switching frequency of the power MOSFET switches, causing an efficiency loss [5-8].

In the paper we propose an original architecture and implementation of an 9-bit hybrid LBDD modulator for digital Class-BD amplifier, using STM32 microcontroller with its peripherals, and additionally two integrated 3-bit programmable tapped delay lines (PTDLs).

This paper is organized as follows: Section 2 presents the general concept of the 9-bit hybrid LBDD modulator, describes system clock selection and timing requirements to synchronize different parts of the modulator and presents linearized LBDD algorithm. Section 3 presents the architecture of the proposed modulator and the design of the DTC circuit using PTDL. Section 4 presents simulation and measurement results. The overall conclusions are given in Section 5.

II. General Concept of the Linearized 9-Bit Hybrid LBDD PWM Modulator

Similarly to the natural sampled NBDD PWM, the LBDD PWM should also generate two LBDD physical sequences of LBDD PWM pulses to switch the H-bridge MOSFET switches of the Class-BD amplifier. One of these sequences, generating on the base of the discrete PCM data for the direct audio signal, controls the left H-bridge leg, while the second one, generating on the base of the discrete PCM data for the inverted audio signal, controls the right H-bridge leg [1-3, 11-14]. Therefore, architecture of the LBDD modulator may be composed of two synchronous linearized Class-AD double sided (LADD) PWM subsystems, converting at the same time direct and inverted audio signals, in the same way as is shown in Fig.1b,c.

The direct and inverted audio input signals are converted into two 12-bit PCM data streams, then are directly transformed into 32-bit LBDD DPWM data of the pulse-edge locations within *n*-th period of the switching frequency and next requantized to the 9-bit digital outputs. Finally, requantized 9-bit pulse-edge locations are converted by the DTCs into the two physical trains of 1-bit LBDD PWM pulses, to control the H-bridge MOSFET switches.

A. System Clock Selection and Timing

The DTC with N_{rq}-bit resolution, based on counter method in down counting mode, requires clock frequency [11-16]:

$$f_{CLK} = f_c \times 2^{N_{rq}+1} \tag{1}$$

giving time resolution of generated pulse:

$$\Delta t_{min} = \frac{T_{CLK}}{2} \tag{2}$$

where f_c is the switching frequency of the H-bridge MOSFET switches.

To moderate an excessive requirement of high clock frequency, instead of poor counter method, the hybrid method is used [11-18]. The hybrid quantizer converts the MSB) $[(N_{rq} - 1) : m]$ data using counter method, while the remaining part of the LSB $[(m - 1) : 0]$ data using a quantizer system based on the PTDL.

Hybrid N_{rq}–bit LADD modulator, processing the data of $(N_{rq} - m)$ MSBs on the base the counter method, requires clock frequency f_{CLKh} [12-16]:

$$f_{CLKh} = f_c \times 2^{(N_{rq}-m)+1} \tag{3}$$

The quantizer processing the LSB (2:0) data comprises a cascade of 2^m identical delay segments, with the same delay time [12-16]:

$$t_{d1} = \frac{T_{CLKh}}{2^m} \tag{4}$$

In our design of 9-bit hybrid LBDD PWM, each of two synchronous hybrid DTCs converts 6 MSB (8:3) data using TIM1 and TIM8 timers with advanced control of the microcontroller, while the remaining 3 LSB (2:0) data - using a quantizer system based on the integrated 3-bit FAST TTL PTLD.

The clock selection and timing of all signal processing blocks are based on the maximum frequency of the three microcontroller AHB buses: f_{osc} = 168 MHz [19].

According to the equations (3, 4), the clock frequency of the high-speed APB2 domains (connecting utilized peripheral devices such as TIM1, TIM8, ADC) and also the clock frequency of the external quantizer system based on the 3-LSB (2:0) PTDL, has been set at:

$$f_{PCLK2} = f_{CLKh} = \frac{f_{osc}}{P_1} = \frac{168\ \text{MHz}}{4} = 42\ \text{MHz} \tag{5}$$

The total ADC conversion time T_{CONV} [19] has been set at the same time as the switching period T_c, to avoid interpolation of the PCM audio data stream sampled at the

frequency f_c and to save significantly computation time. The peripheral ADC of the STM32F407xx microcontroller system has 16 multiplexed channels and it is possible to organize the conversions in two groups: regular and injected [19]. According to equation (3), to receive $T_{CONV} = T_c = 128T_{CLKh}$, a regular group of five conversions has been composed selecting in the ADC_SQRx registers of the regular channels as well their order in the conversion sequence and writing total number of conversions in the regular group of the L[3:0] bits in the ADC_SQR1 register.

$$T_{CONV} = \sum_1^G \text{Sampling time} + 12 \text{ cycles} = \\ = 4 \times 15T_{CLKh} + 68T_{CLKh} = 128T_{CLKh} \quad (6)$$

So, the ADC generates the PCM audio data stream with frequency:

$$f_{CONV} = f_c = \frac{f_{CLKh}}{2^{(N_{rq}-m)+1}} = \frac{42 \text{ MHz}}{2^7} = 328{,}125 \text{ kHz}$$

$$T_{CONV} = T_c = \frac{1}{f_c} = \frac{1}{42\text{MHz}} \times 128 = 3{,}0762\mu s \quad (7)$$

$$\text{and: } t_{d1} = \frac{T_{CLKh}}{2^m} = \frac{23{,}81}{2^3} = 2{,}97\text{ns}$$

1) Piecewise Linear Approximation of Double Sided LBDDPWM

Generated by ADC discrete PCM samples at $f_{CONV} = f_c$ frequency are further interpolated by calculation of Q intermediate evenly distributed PCM samples. Fig. 2 shows an example for odd $Q = 5$. Using the border and new samples, we receive piecewise linear approximation of the digital audio input signal.

Solving the crossing points between the triangular carrier signal and the approximated signal we obtain the PWM pulse-edge locations $t_p(n)$ and $t_k(n)$ within n-th period of the switching frequency (the positions of the leading edge and the trailing edge, appropriately).

In the first period T_c of the switching frequency, the triangular signal is described by the equations:

$$s_f = -\frac{4}{T_c}\bar{t} + 1; \text{ for: } 0 \le \bar{t} < \frac{T_c}{2} \quad (8)$$

$$s_r = \frac{4}{T_c}\bar{t} - 3; \text{ for: } 0 \le \bar{t} < T_c \quad (9)$$

In the first step of the algorithm, the necessary values of the normalized triangular signal are calculated and stored for the same time points, where Q intermediate samples are evenly distributed at the following distances :

$$\text{For even } Q \Rightarrow k = 1, 2, .., \frac{Q}{2}$$

$$S_{f,0} = 1 \; ; \; S_{f,k} = \frac{-4k}{Q+1} + 1 \; ; \; S_f\left(\frac{T_c}{2}\right) = -1 \quad (10)$$

$$S_{r,(Q/2)}\left(\frac{T_c}{2}\right) = -1 \; ; \; S_{r,\left(\frac{Q}{2}\right)+k} = \frac{4\left[\left(\frac{Q}{2}\right)+k\right]}{Q+1} - 3, \; S_{r,(Q+1)} = 1$$

$$\text{For odd } Q \Rightarrow k = 1,2,\ldots, (Q-1)/2$$

$$S_{f,0} = 1 \; ; \; S_{f,k} = \frac{-4k}{Q+1} + 1 \; ; \; S_{f,\,(Q-1)/2+1} = -1 \quad (11)$$

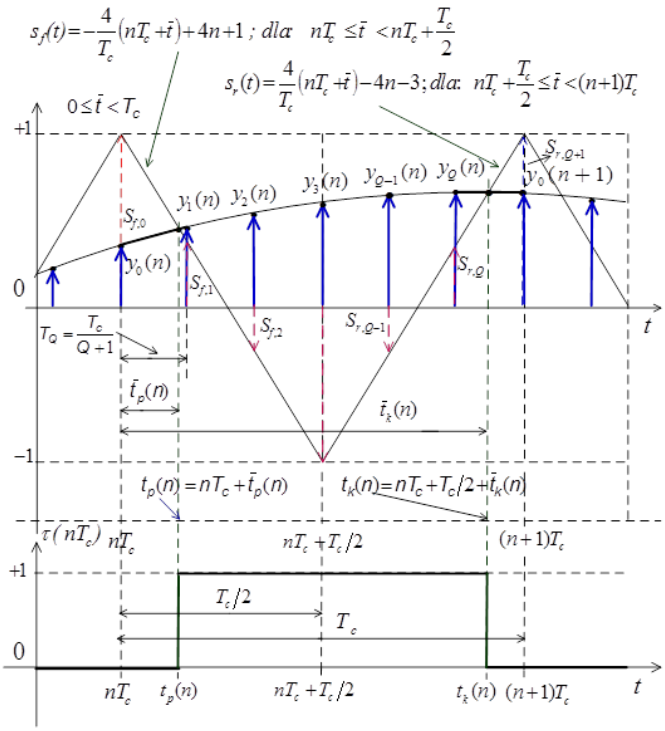

Fig.2. Piecewise linear approximation of the digital audio input ($Q = 5$)

$$S_{r,((Q-1)/2)+1} = -1 \; ; S_{r,\left(\frac{Q-1}{2}\right)+k} = \frac{4[Q-1)/2 + k]}{(Q-1)} - 3$$

$$S_{r,(Q+1)} = 1$$

Using a successive comparison method, we should find i-th range between $y_i(n)$ and $y_{i+1}(n)$ samples in which:

$$y_i(n) < S_{f,i} \; ; \; y_{i+1}(n) > S_{f,i+1}; \text{ for } 0 \le i < \frac{Q}{2} + 1 \text{, for even } Q$$

$$y_i(n) < S_{f,i} \; ; \; y_{i+1}(n) > S_{f,i+1}; \text{ for: } 0 \le \text{i} \le \frac{Q-1}{2} + 1, \quad (12)$$

for odd Q

A straight line passing through coordinates of two points: $\frac{iT_c}{Q+1}$, $y_i(n)$ and $\frac{(i+1)T_c}{Q+1}$, $y_{i+1}(n)$ intersects the trailing edge of the triangular signal in a point determining the leading edge location $\bar{t}_p(n)$ of the PWM pulse within n-th period of the switching frequency (Fig.2).

Successive computation for all values of $n = 0, 1, 2, \ldots, (N-1)$, gives:

$$t_p(n) = nT_c + \bar{t}_p(n) = nT_c + \frac{T_c[1 - y_0(n)]}{4 + 2[y_1(n) - y_0(n)]}, \quad (13)$$

at: $V_T = 1\text{V}$.

It is however possible, that for larger value of the modulation index M $(M < 1)$, there are no: $i < \frac{Q}{2} + 1$ satisfying an inequalities (12) for even Q, because the two adjacent $y_i(n)$ and $y_{i+1}(n)$ samples are located in the two separate ranges of the trailing and leading edges of the triangular signal, what is shown in Fig. 3.

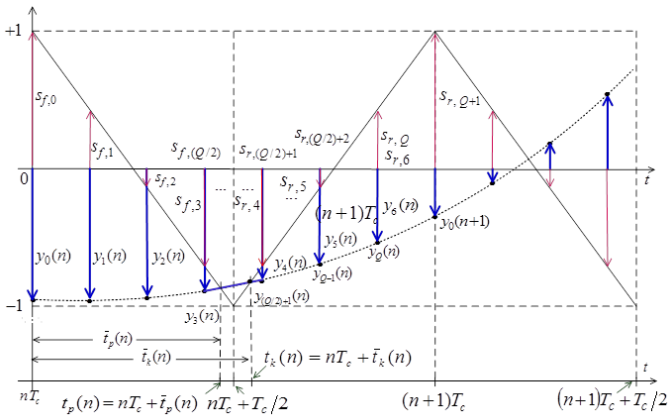

Fig.3. Piecewise linear approximation of the digital audio input (Q = 6)

In this case, the approximating straight segment is passing through coordinates of two points:

$$\frac{\left(\frac{Q}{2}\right)T_c}{Q+1},\ y_{\left(\frac{Q}{2}\right)}(n) \quad \text{and} \quad \frac{\left[\left(\frac{Q}{2}\right)+1\right]T_c}{Q+1},\ y_{\left(\frac{Q}{2}\right)+1}(n) \quad ,$$

which intersects the trailing edge of the triangular signal in a point determining the critical leading edge location $\bar{t}_{cp}(n)$ of the PWM pulse:

$$t_k(n) = nT_c + \bar{t}_k(n) = nT_c + \frac{T_c[y_2(n)-2y_1(n)-3]}{2[y_2(n)-y_1(n)]-4}, \tag{14}$$

at: V_T = 1V.

Very similarly, we can calculate the trailing edge $\bar{t}_k(n)$ of the PWM pulse. Using now equation (8), describing leading edge of the triangular signal, after some successive comparison, we can find j-th range between $y_j(n)$ and $y_{j+1}(n)$ samples in which:

$$y_j(n) > S_{r,j}\,;\ y_{j+1}(n) < S_{r,j+1}\,, \text{for } \frac{Q}{2}+1 \le j < Q+1,$$

for even Q. (15)

$$y_j(n) > S_{r,j}\,;\ y_{j+1}(n) < S_{r,j+1}\,, \text{ for } \frac{Q-1}{2}+1 \le j < Q+1,$$

for odd Q. (16)

A straight line passing through coordinates of two points: $\frac{jT_c}{Q+1}$, $y_j(n)$ and $\frac{(j+1)T_c}{Q+1}$, $y_{j+1}(n)$ intersects the leading edge of the triangular signal in a point determining the trailing edge location $\bar{t}_k(n)$ of the PWM pulse within n-th T_c period.

Successive computation for all values of $n = 0, 1, 2,\ldots,(N-1)$, gives:

$$\bar{t}_k(n) = \frac{T_c[jy_{j+1}(n)-(j+1)y_j(n)-3]}{[y_{j+1}(n)-y_j(n)](Q+1)-4} \tag{17}$$

$$t_k(n) = nT_c + \bar{t}_k(n) \tag{18}$$

As well in this case, for even Q and larger value of the modulation index M, there are no: $j < Q+1$ satisfying an inequalities (16), because the two adjacent $y_j(n)$ and $y_{j+1}(n)$ samples are located in the two separate ranges of the trailing and leading edges of the triangular signal.

In the same way as for the critical leading edge location $\bar{t}_{cp}(n)$, we can define the critical trailing edge location $\bar{t}_{ck}(n)$ of the PWM pulse:

$$\bar{t}_{ck}(n) = \frac{T_c\left\{\left(\frac{Q}{2}\right)y_{\left(\frac{Q}{2}\right)+1}(n)-\left[\left(\frac{Q}{2}\right)+1\right]y_{\frac{Q}{2}}(n)-3\right\}}{\left[y_{\left(\frac{Q}{2}\right)+1}(n)-y_{\frac{Q}{2}}(n)\right](Q+1)-4} \quad \text{and}$$

$$t_{ck}\ (n) = nT_c + \bar{t}_{ck}\,(n) \tag{19}$$

Practically, to provide the *THD* under 0.1 % (higher Q results in lower *THD*) within the audio baseband and modulation index $0 \le M \le 1$, the Q coefficient may be Q = 1, 2 or 3 .

Because the calculations of the edge locations $t_p(n)$ and $t_k(n)$ for even Q is more complicated it is appropriate to make an assumption that Q is odd and equals 1 or 3. This assumption results in a very simple computationally algorithm providing easy-going real-time calculation of the DPWM signals.

For $Q = 1$, between two adjacent samples $y_0(n)$ and $y_2(n)$ only one intermediate sample $y_1(n)$ is generated with the distance: $T_Q = \frac{T_c}{2}$, and the pulse-edge locations $t_p(n)$ and $t_k(n)$ are determined by the equations:

$$t_p(n) = nT_c + \bar{t}_p(n) = nT_c + \frac{T_c[1-y_0(n)]}{4+2[y_1(n)-y_0(n)]} \tag{20}$$

$$t_k(n) = nT_c + \bar{t}_k(n) = nT_c + \frac{T_c[y_2(n)-2y_1(n)-3]}{2[y_2(n)-y_1(n)]-4} \tag{21}$$

For $Q = 3$, between two adjacent samples $y_0(n)$ and $y_4(n)$ three intermediate sample: $y_1(n)$, $y_2(n)$, $y_3(n)$ are generated with the distance: $T_Q = \frac{T_c}{4}$, and the pulse-edge locations $t_p(n)$ and $t_k(n)$ are determined by the equations:

$$t_p(n) = nT_c + \bar{t}_p(n) = nT_c + \frac{T_c[1+iy_{i+1}(n)-(i+1)y_i(n)]}{4+4[y_{i+1}(n)-y_i(n)]} \tag{22}$$

where: if $y_0(n) < 1$ and $y_1(n) > 0$, then $i = 0$,

if $y_1(n) < 0$ and $y_{21}(n) > -1$, then $i = 1$

$$t_k(n) = nT_c + \bar{t}_k(n) = nT_c + \frac{T_c[jy_{j+1}(n)-(j+1)y_j(n)-3]}{4[y_{j+1}(n)-y_j(n)]-4} \tag{23}$$

where: if $y_2(n) > -1$ and $y_3(n) < 0$, then $j = 2$,

if $y_3(n) > 0$ and $y_4(n) > 1$, then $j = 3$

Real-time calculations of the pulse-edge locations , both for the original audio signal: $t_p^l(n)$ and $t_p^l(n)$ are well for the inverted one: $t_p^r(n)$ and $t_k^r(n)$, should be calculated within each n-th T_c period of the switching frequency.

The calculated N_q-bit locations of the leading edge $t_p(n)$ and trailing edge $t_k(n)$ (calculated from the above equations for the direct and inverted audio input signals, and indexed by l and r respectively) should be requantized to a lower N_{rq}-bit output resolution ($N_{rq} < N_q$). However, the truncation of the digital input data to N_{rq} -bits results in higher quantization noise floor in the audio bandwidth (BW). i.e. lower Signal to Quantization Noise Ratio (SQNR).The requantizing process increases the SQNR within the audio BW and moves the quantization noise power to an unused part of the bandwidth created by oversampling [9, 10]. A recursive noise shaping models with one or two feedback loops are shown in Fig. 4 a,b, in which the quantizer is modeled as an additional, independent added noise source [10].

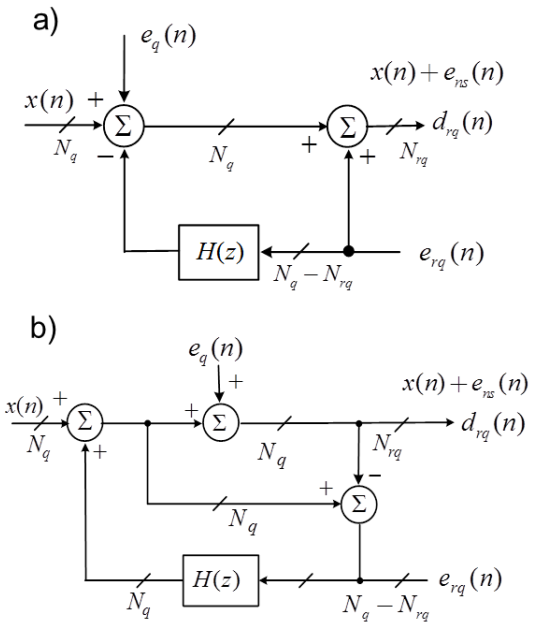

Fig. 4. Two architectures of a recursive noise shaping model, modeled as added noise source: a) with 1 feedback loop, b) with 2 feedback loops.

There are the following variables in the model:

$x(n)$ - digital input (calculated N_q-bit pulse-edge locations: $t_p^l(n), t_k^l(n), t_p^r(n), t_k^r(n)$),

$e_q(n)$ - quantization error on input (independent added noise source),

$e_{rq}(n)$ - requantizing noise source (generating after the truncation of the calculated N-bit digital data to N_{rq}-bit resolution),

$e_{ns}(n)$ - requantized noise on output (after the noise shaping requantizing process),

$d_q(n) = x(n) + e_q(n) + e_n(n)$ - noisy digital output (calculated N_{rq}-bit pulse-edge locations: $t_p^l(n), t_k^l(n), t_p^r(n), t_k^r(n)$,

$H(z)$ - n-th order FIR filter with integer coefficients.

The different word lengths of processed data are also marked in the Fig. 4.

Assuming that the error sequence $e_q(n)$ is modeled as uniformly distributed white noise and is uncorrelated with the signal sequence $d_{rq}(n)$, on the base the model with 2 feedback loops in Fig.4b, we can obtain the following z-domain relationship between the input - output of the system.

$$D_{rq}(z) = X(z) + E_{ns}(z) \tag{24}$$

$$E_{rq}(z) = X(z) + E_{rq}(z)H(z) - [X(z) + E_{ns}(z)] \tag{25}$$

Based on equations (24, 25), we obtain the relationship between the quantization noise source - represented by error noise $e_q(n)$ - and the requantized noise source $e_{ns}(n)$, defined as noise transfer function $NTF(z)$.

$$NTF(z) = \frac{E_n(z)}{E_{rq}(z)} = 1 - H(z) \tag{26}$$

We get the same relationship (26) for the simpler model with 1 feedback loop, presented in Fig.4a.

The noise shaping filter $H(z)$ requires at least one sample delay, i.e. transmittance $H(z)$ can be factorized in a one sample delay and a normal causal digital filter. In our design, a fifth order noise shaping transfer characteristic $NTF(z)$ has been applied:

$$NTF(z) = c_0 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4} + c_5 z^{-5} \tag{27}$$

with: $c_0 = -1$; $c_1 = 5$; $c_2 = -10$; $c_3 = 10$; $c_4 = -5$; $c_5 = 1$

The noise shaping process based on the model with 2 feedback loops achieves much lower *SNR* level within the audio baseband, however it requires higher computational power.

III. Architecture of the Hybrid LBDD DPWM Circuit Using PTDL

Architecture of the hybrid LBDD DPWM is composed of two synchronous hybrid LADD DPWMs. The first of them $LADD_L$ DPWM generates sequences of $LADD_L$ PWM pulses (on the base the direct audio signal) to control MOSFETs of the left H-bridge leg, while the second $LADD_R$ DPWM generates sequences of $LADD_R$ PWM pulses (on the base the inverted audio signal) to control MOSFETs of the right H-bridge leg. Because $LADD_L$ PWM and $LADD_R$ PWM circuits are similar, they can be implemented in the same way.

The following description applies only to modulator $LADD_L$ PWM. The calculated data of the leading edge $t_p^l(n)$ and trailing edge $t_k^l(n)$ locations of the $LADD_L$ PWM impulse are requantized to the lower 9-bit resolution, next they are divided into the two parts of 6 MSB(8:3) bits and 3 LSB(2:0) bits of the data and sequentially are rewritten into LADDL registers:

The hybrid quantizer converts 6 MSB: $d(8:3)$ using counter method, based on the STM32 microcontroller and its advanced-control timers TIM1 or TIM8, while the remaining 3 LSBs: $d(2:0)$ - using a method based on the integrated 3-bit FAST TTL PTLD [20].

The PTDL comprises a cascade of N = 8 identical delay cells, with a delay time $t_{d1} = 2{,}97$ns, defined by equation 3.

Fig. 5a shows logical scheme of the $LADD_L$ sub-circuit, converting 3-LSB (2:0) bits of the data, using the method based on the 3-bit PTDL, and Fig. 5b shows time domain waveforms of the control and output signals to illustrate the principle of operation.

Using 6 MSB(8:3) bits of the leading edge $t_p(n)$ and trailing edge $t_k(n)$ locations of the $LADD_L$ DPWM data, firstly two linearized Class-AD single sided LADS DPWM impulses are generated in each n-period T_c of the switching frequency.

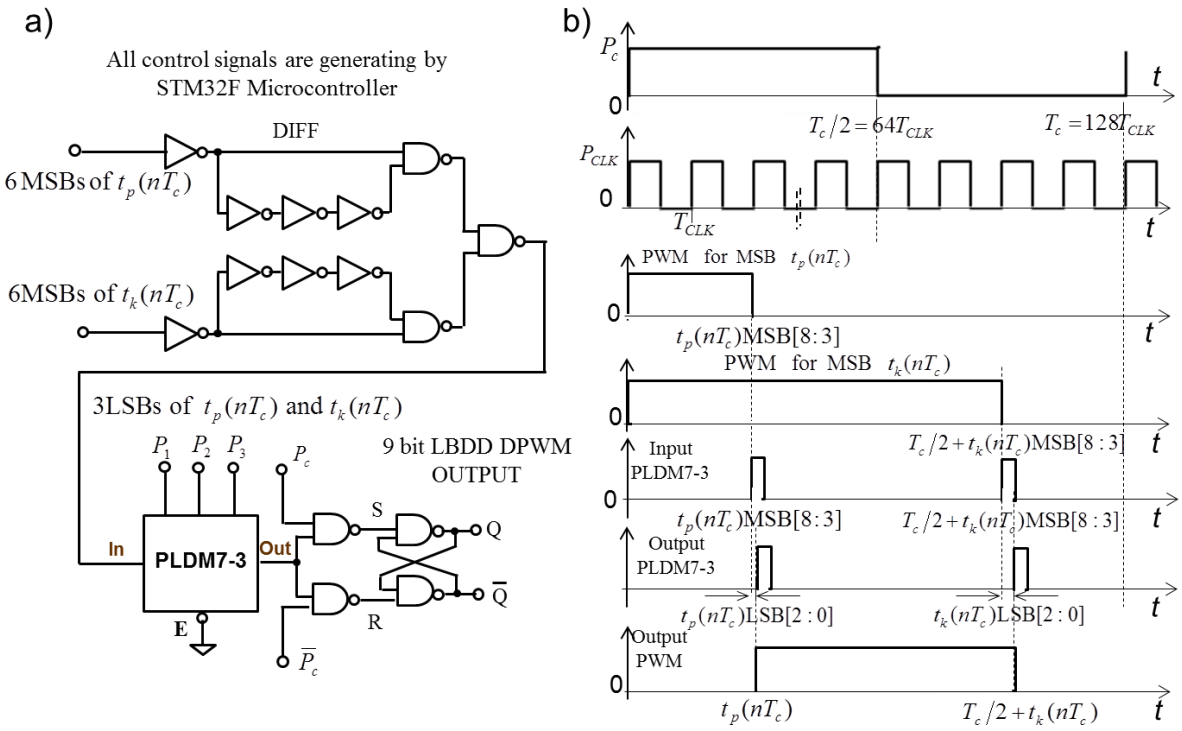

Fig.5. Logical scheme of the sub-LADDL circuit, converting 3-LSB bits using 3-bit PTDL (a) and time domain waveforms of the control and output signals (b).

The rising edges of both pulses start at the beginning of the T_c period, while the falling edge appears at the leading edge $t_p(n)$ location for the first impulse, and at the trailing edge $t_k(n)$ location for the second one. A timer TIM1 was used to generate these waveforms.

The falling edges of both generated pulses are differentiated and then passed through a 3-bit PTDL. At the output of PTDL we get the pulses delayed in time determined by the programming 3 LSB(2:0) bits of the leading edge $t_p(n)$ and trailing edge $t_k(n)$ locations of the $LADD_L$ DPWM impulse. This requires to program twice the PTDL in each switching period nT_c. At the beginning of the period nT_c, we have to program the PTDL by the 3 LSB(2:0) bits of the leading edge $t_p(n)$ locations and hold these data by the first half $T_c/2$ period, while at the beginning of the second half $T_c/2$ period by the 3 LSB (2:0) bits of the trailing edge $t_k(n)$ locations and hold these data by the second half $T_c/2$ of the period.

The output flip-flop is setting by the delated impulse corresponding to the leading edge $t_p(n)$ locations and resetting by by the delated impulse corresponding to the trailing edge $t_k(n)$ locations, therefore on the flip-flop output final 9-bit $LADD_L$ DPWM signal is generating.

Similarly to that described above, we receive the final 9-bit $LADD_R$ DPWM signal generating for the inverted audio signal. The difference between $LADD_L$ DPWM and $LADD_R$ DPWM results as LBDD DPWM output signal.

IV. Simulation and Measurement Results

The time domain waveforms and frequency spectrum characteristics of DPWM signals have been simulated using Matlab ® tools. The frequency spectrum has been estimated by storing a number of pulses of the LBDD DPWM output signal, which represents at least one period of the modulating waveform.

Fig. 6 shows simulated results of time waveforms (a) and frequency spectrum of the 32-bit LBDD DPWM output before requantizition (b) and the 9-bit LBDD DPWM output after requantizition, using recursive model of noise shaping architecture with 2 feedback loops and described in the paper LPWM algorithm (c) for: $M = 0.95$, $f_c = 328.125$ kHz, $f_m = 10$ kHz, $Q = 1$, where M – modulation index, Q – number of intermediate PCM audio samples during the interpolation within period T_c, f_c – switching frequency, and f_m – frequency of the modulating audio signal.

Simulations of *THD* coefficients of the LBDD DPWM signal, for two architectures of recursive noise shaping model, as well as a comparison of *THD* coefficients resulting for LBDD, NBDD and UBDD modulations, are shown in Fig. 7.

Figs. 7 a, b show *THD* coefficients of the LBDD DPWM signal, at: $Q = 1$, two modulating frequencies: $f_{m1} = 10$ kHz, $f_{m2} = 20$ kHz, and two architectures of recursive noise shaping model: a) with 1 feedback loop, b) with 2 feedback loops.

This comparison indicates that even a simple LBDD algorithm (at $Q = 1$) and noise shaping process using recursive noise shaping model with 2 feedback loops allows a significant improvement in the modulator's linearity. Furthermore, by introducing a larger number Q of intermediate PCM audio samples within period Tc, we can further reduce the THD level

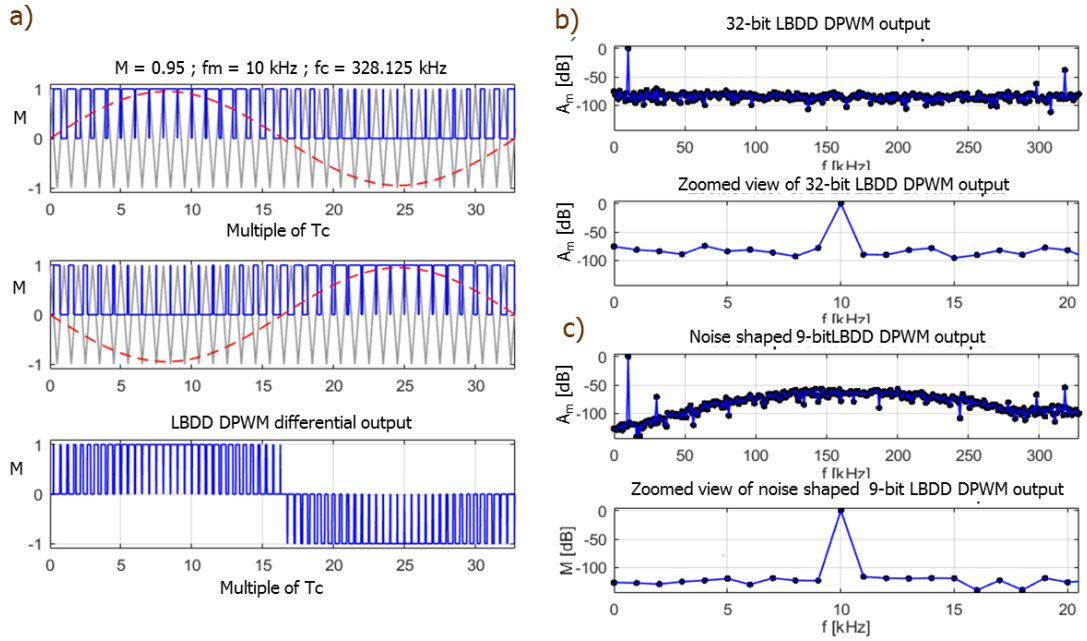

Fig. 6. Simulation results in Matlab; Time domain waveforms of LBDD DPWM (a) ; Frequency spectrum of the LBDD DPWM output at: M = 0.95, f_c = 328.125 kHz, f_m = 10 kHz for Q = 1; before requantizition (b), after requantizition to the 9-bit output data (c).

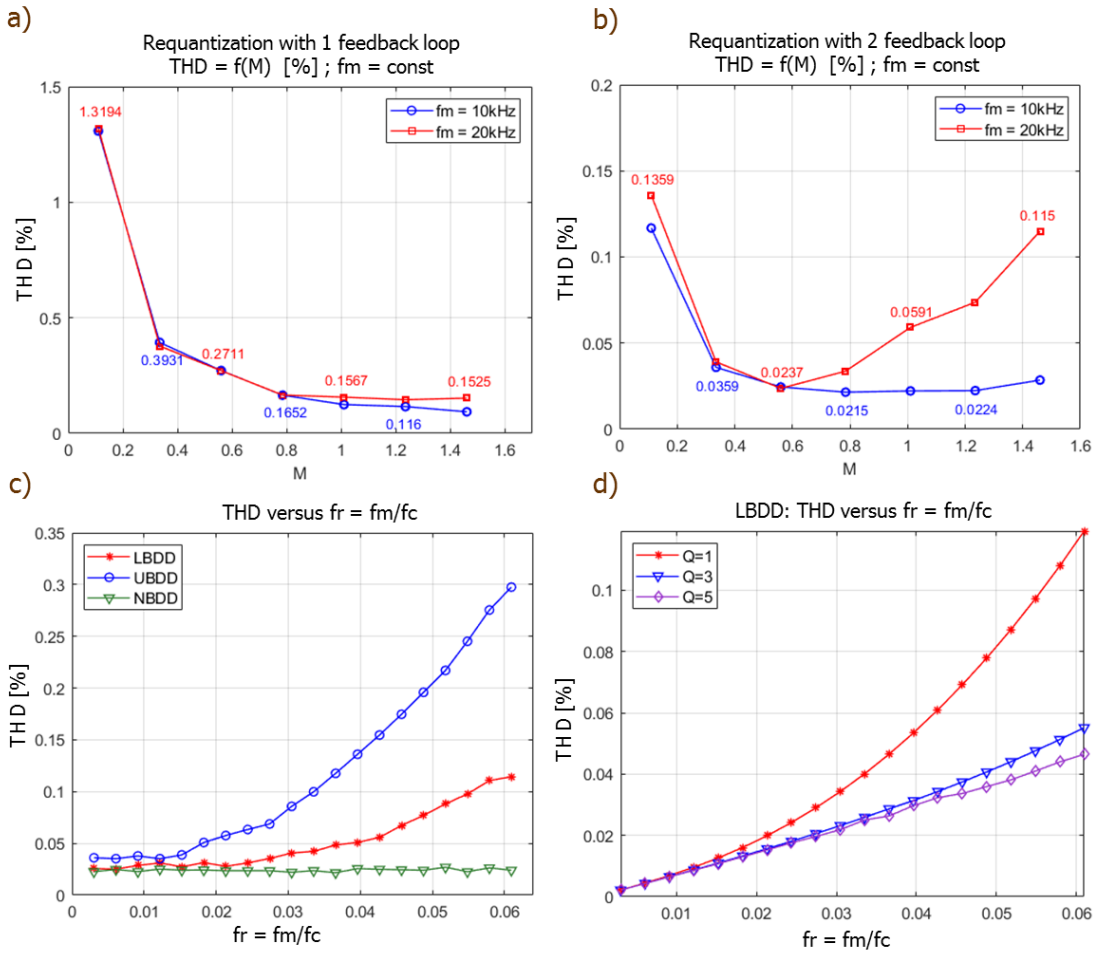

Fig. 7. Simulation results; *THD* coefficients on the LBDD DPWM output, at: Q =1, two modulating frequencies: f_{m1} = 10 kHz, f_{m2} = 20 kHz, and two architectures of recursive noise shaping model: a) with 1 feedback loop, b) with 2 feedback loops ; Comparison of *THD* coefficients for NBDD, UDDD and LBDD modulators (d) ; *THD* of the LBDD DPWM output versus $f_r = f_m/f_c$, for different Q values.

of the LBDD DPWM signal and approach the *THD* level of the optimal analog NPWM modulator. This conclusion is confirmed by the characteristics of *THD* coefficients for NBDD, UDDD and LBDD modulators versus $f_r = f_m/f_c$, shown in Fig. 7c, as well *THD* coefficients of the LBDD DPWM output versus $f_r = f_m/f_c$, for different Q values (Fig. 7d).

Oscillograms of two 6-MSB LADS DPWM pulses generating on the base counter method, using STM32 microcontroller and its peripherals, are shown in Fig. 8 (from the top).

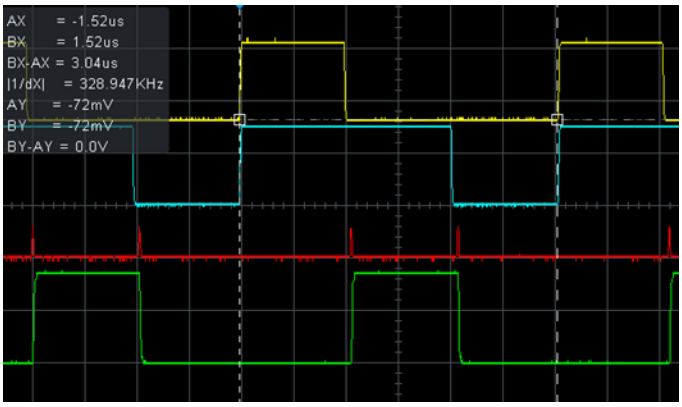

Fig. 8. Oscillograms of two 6-MSB LASS DPWM impulses generating on the base counter method (from top) ; Generation of 6-MSB $LADD_L$DPWM impulses on the flip-flop output of the $LADD_L$ modulator (from down).

The falling edges of both 6-MSB LADS DPWM pulses are differentiated and passed through the 3-bit PTDL, then used to set and reset the output flip-flop, what illustrates oscillograms in Fig.8 (from down).

Fig.9 shows oscillograms of the time waveforms generated on the 9-bit hybrid $LADD_L$ DPWM, $LADD_R$ DPWM and LBDD DPWM output signals (from top to down, respectively).

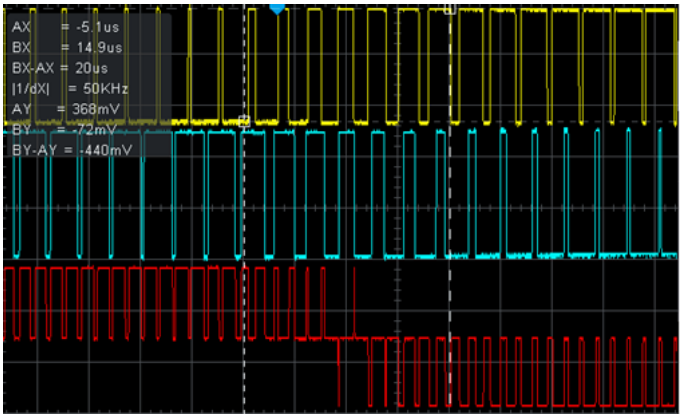

Fig.9. Oscillograms of the time waveforms generated on the 9-bit hybrid $LADD_L$ DPWM, $LADD_R$ DPWM and LBDD DPWM outputs (from top to down, respectively).

$LADD_L$ DPWM controls MOSFET switches of the left H-bridge leg, while $LADD_R$ DPWM controls MOSFET switches of the right H-bridge leg, resulting the LBD PWM output signal at the H-bridge DM output.

Reference time waveform generated on the output of the LBDD DPWM modulator has been used to measure spectral and *THD* characteristics, presented in Fig. 10.

V. Conclusions

A new and original architecture as well implementation of 9-bit Linearized Pulse Width Modulator circuit for digital Class-BD power amplifier has been proposed. Full LBDD DPWM processing algorithm has been implemented on the base the hybrid method using STM32 microcontroller with its peripherals, and additionally two generally available catalog 3-bit programmable tapped delay lines.

Extensive verification of algorithm and circuit operation as well as simulation in MATLAB and experimental results of the proposed 9-bit hybrid LBDD DPWM circuit have been performed. Comparison of *THD* coefficients simulated in MATLAB and presented in Fig.7 a, b indicates, that even a simple LBDD algorithm (at Q = 1) using recursive noise shaping model with two feedback loops allows a significant improvement in the modulator's linearity compared to other types of DPWM. For higher Q values, LBDD modulator can further reduce *THD* levels, approaching the optimal analog NBDD modulator.

6-MSB converter based on the counter method, uses relatively simple circuit implementation and exhibits perfect linearity of the digital to time conversion. For this purpose, all functional blocks in the system must be perfectly synchronized, as well the T_c switching period in both $LADD_L$ DPWM and $LADD_R$ DPWM subsystems must start at the same time.

Presented in the paper original 3-LSB converter using integrated 3-bit programmable PTDL is also very simple and has high processing accuracy. All programmable delay times ”step to step” of the PTDL are referenced to ”step zero”, which is referenced to the input pin. The delay time at step zero is 5 ns, but it has no effect on the processing accuracy, because all leading edge $t_p(n)$ and trailing edge $t_k(n)$ locations of the physical train of 1-bit LBDD DPWM impulses are delayed for the same 5 ns time.

The practically measured *THD* level at the output of the LBDD modulator (characteristic $THD = f(f_m)$ presented in Fig. 10.d), have a bit higher level than that obtained in the Matlab simulation (Fig.6d, for Q = 1). However from a practical point of view, they are quite satisfactory, providing *SNR* of 80 dB and *THD* lower then 0,3% within the audio baseband up to 20 kHz.

The advantage of the digital DPWM modulator is also the easy programming of the appropriate dead time at the rising edges of all signals driving the power stage MOSFETs, which allows approximately to achieve zero voltage switching and to prevent shoot-through currents.

A unique advantage of the proposed 9-Bit LBDD DPWM for Digital Class-BD Amplifier is that it’s basic configuration is very simple, can be implemented using only STM32 microcontroller, two generally available catalog 3-bit programmable tapped delay lines and some standard logic gates.

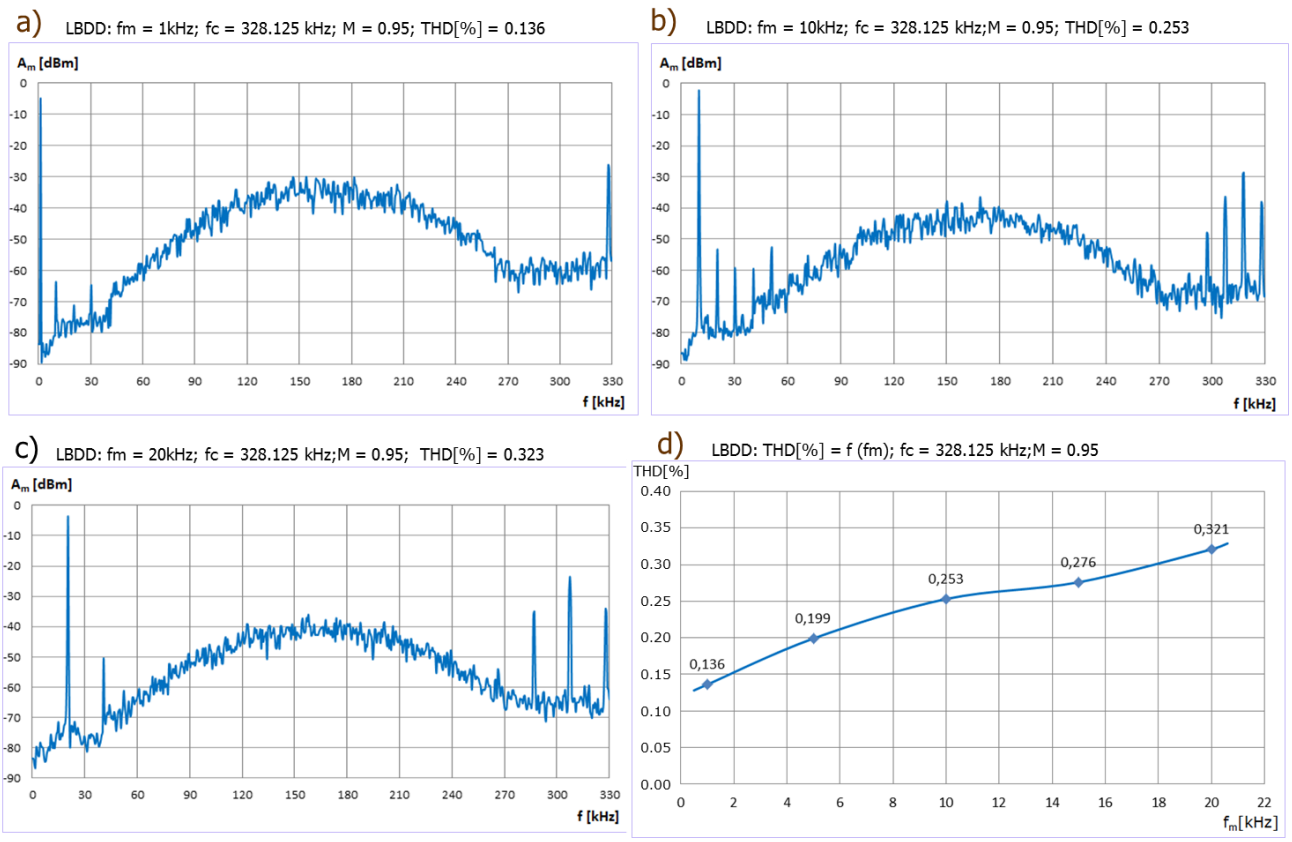

Fig. 10. Spectral characteristics measured on the hybrid 9-bit LBDD DPWM output, at the modulation frequency: a). f_{m1} = 1 kHz, b). f_{m2} = 10 kHz, c). f_{m3} = 20 kHz, d) *THD* versus f_m characteristic.

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