Trends in hybrid pixel detectors for X-ray imaging using deep submicron VLSI technology

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The article covers the latest developments in pixel detectors used for X-ray imaging as well as the description of the practical solution – a multichannel integrated circuit dedicated to X-ray imaging. In general introduction a wide range of pixel detector applications is presented. The main part focuses on the challenges and new solutions for the field of X-ray imaging, including 3D integration, silicon-on-insulator and submicron technologies. Since minimization of a pixel size together with implementing more functionality are important issues in the detectors' and integrated circuits' design, the aspects of channel-to-channel uniformity and additional effects like charge sharing between pixels are taken into consideration. In the last section, the Authors present the application specific integrated circuit designed in 40 nm technology dedicated to X-ray detection and future prospects are discussed.

Key words: X-ray imaging, hybrid pixel detectors, 3D technologies, SOI technologies

Introduction

The development of multichannel detectors consisting of millions of pixels plays a crucial role in the fast advance in the particle physics. Nowadays, experimental techniques allow measuring precisely the parameters of the particle hit such as the direction and the energy of the particles produced during the collisions at high-energy accelerators. This kind of application requires dedicated integrated circuits which provide fast processing, good spatial resolution and ability to detect the particles precisely, even in harsh radiation environment [1].

The mastering of the pixel detectors used in the particle physics has also led to the development of the new fields of applications such as crystallography, astrophysics, clinical dosimetry or medicine, where pixel detectors may replace older conventional techniques [1,2].

In the protein X-ray crystallography high counting rate and high dynamic range of the device are necessary to register diffracted X-ray beams and by that means identify the protein crystal structure. Imaging using pixel detectors gives the information about the material structure and its disorders, and that is why it is widely used in many areas of industry and science such as biotechnology and pharmaceutical industry just to name a few [1].

Another example of X-ray pixel detectors' application is medical imaging. For a long time X-ray images were taken using a film, but nowadays applying pixel detectors working in single photon counting mode allow distinguishing between the photons with different energies. Since various materials or tissues absorb X-ray of different energy levels, selective multi-energy imaging is a solution for precise imaging and tissue differentiation (for example soft tissues and bones) [3].

Development trends – design aspects

Taking into account medical applications, such as real time radiology or radiography with distinction of radiolabels, pixel detectors and the readout electronics need to be designed to satisfy certain requirements: small pixel size – to improve spatial resolution, low noise – to enhance image quality, small analog parameters' spread – to improve image homogeneity, fast processing – to reduce time of patient exposure to the radiation. Keeping the balance between these, often contradictory, limitations, is the designer's task.

Typically, the detector system consists of the sensor (often made of Si, Ge, CdZnTe depending on application), in which the interaction with radiation takes place, and the readout chip combined with the sensor by bump-bonding. The readout integrated circuit is responsible for signal acquisition, processing, control and data buffering. Exemplary scheme of chip's building blocks is presented in further part of article. The active area of the chip contains matrix of pixels with the same functionality each, including: charge sensitive amplification, signal shaping and discrimination. Standard readout electronics path is presented in Figure 1.

Maintaining full functionality of the pixel and at the same time meeting all the design requirements aforementioned, often leads to the development of new research directions. A few of them are presented below.

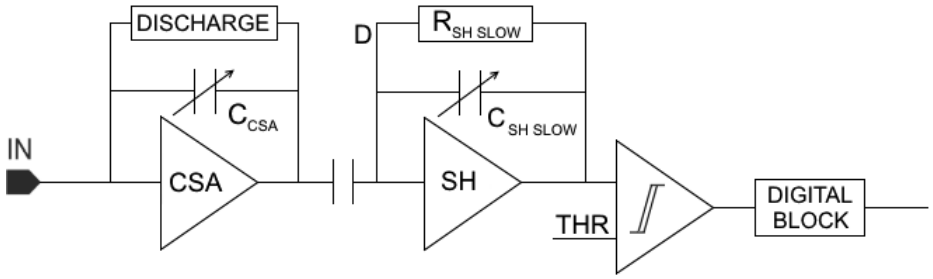

Figure 1. Exemplary readout channel architecture including charge sensitive amplifier, shaper, discriminator and digital block

3D integration

3D integration is a technique in which integrated circuits are produced in the bonding process and two or more wafers are connected with through-silicon-vias (TSV). It allows to obtain readout chips without dead space and consequently edgeless detectors can be produced which is especially important for large-area detectors with many channels and complex processing [4]. Although, there are various advantages of 3D integration like reducing power consumption and improving its distribution, fitting the functionality in smaller pixel or reducing the average wire length (which allows higher speeds and lowers noise), taking the full advantage of this method requires sophisticated design techniques and designer's experience. The reason is that chips designed for 3D integration must be almost perfectly symmetric so that they can be connected together and work properly afterwards.

Manufacturing of 3D integrated circuits requires some additional stages, like wafer thinning, aligning and fusion bonding [5,6]. Each of these steps raises costs significantly and what is more can introduce errors, reducing yield as a consequence. The manufacturing process currently takes also more time than 2D IC, since more manufacturing steps are involved. As the technology will be more mature all this shortcomings will have less importance.

SOI technology

Another trend in the development of pixel systems is silicon-on-insulator (SOI) technology. In this case, a thin layer of silicon in which transistors are formed is isolated from an active sensor volume by a layer of insulator, usually silicon dioxide. The advantages of this solution are increased switching speed, reduction of current leakage, high gain that may be achieved even in small pixel area [7]. What is also important for large-scale detectors, the technology is less vulnerable to soft errors and signal noise may be reduced. Although this solution is still under development and is now more expensive than standard methods, it may become very attractive in the near future and standard hybrid detectors may be replaced by monolithic SOI devices.

Submicron technologies

In order to achieve better spatial resolution in X-ray imaging, designers tend to minimize the pixel size either maintaining the same functionality or even increasing the functionality of single readout channel.

By reducing transistors' dimensions designer can pack more transistors in the same area which allow implementing aforementioned algorithms. Having more area, two counters instead of one can fit into pixel, which make continuous readout possible. In nearest future it will be possible to place ADC inside pixel which allows measuring hit energy [8].

This trend, however, leads to the problems with uniformity of the channels' analog parameters due to manufacturing imperfections, which are more important as transistors' dimensions are getting smaller. To compensate this effect each pixel contains trimming DAC for each discriminator.

Reducing pixel size also makes the charge sharing effect between pixels more significant, which may result in incorrect energy measurement. That is why correction and charge sharing compensation algorithms ought to be implemented in the chip [9,10].

Additionally technology scaling produces more dense designs which have increased power consumption. Designer could use high Vt transistors (as they have lower leakage currents) or implement other power saving techniques (i.e. clock gating, lower supply voltages or multi voltage domains) to overcome this problem.

Proposed solution

The proposed solution is the application specific integrated circuit designed in 40 nm technology dedicated to X-ray detection. The details of the chip design are described in [11], so this article briefly describes design ideas and focuses mainly on new techniques (such as 3D integration, SOI and submicron technologies) that are or may be applied in the future to our solution.

The analog part of single pixel's front-end electronics comprises of a charge-sensitive amplifier (CSA), two shapers (SH) and two discriminators (DISCR) with 6-bit trimming DACs each (TRIM). Implemented readout electronics path is presented in Figure 2.

The photon hit generates the charge cloud in the detector, the signal is then integrated by CSA which results in the voltage step proportional to the charge generated in the detector. Then the signal is filtered and processed with respect to the timing requirements by the shapers. Considering the submicron technology in which the chip was designed, there is a channel-to-channel transistors' parameter spread because of the inaccuracies in technology process. Thus, trimming DACs were implemented to compensate the nonuniformity of analog parameters, in this particular case the threshold voltage, between channels. Experimental results of analog parameter's trimming proving that correction procedure works properly are presented in Fig.3. The correction was performed on 432 pixels resulting in the decrease of the offset spread.

Moreover, additional functionality for charge sharing effect compensation is also implemented. In submicron technologies with minimizing the pixel size, there is an increase of the probability that the charge cloud generated as a result of photon hit divides between two or more neighbouring pixels' electrodes. This implies that, even though the photon hits the detector in one particular pixel, up to four neighbouring readout channels may register the event. The schematic view of the detector and the charge cloud collected by the pixels is presented in Fig. 4.

Deciding to implement a chip in the latest submicron technology, the designer needs to consider specific algorithm for charge sharing effect compensation. That is why the C8P1 algorithm tested firstly in the simulations [9] was implemented inside the chip. The algorithm output (precise hit position and corrected pulse amplitude) is calculated basing on the information from additional functionality aforementioned implemented in each readout channel: the discriminator checking if the total signal from summing node for four neighbouring pixels is higher than set threshold and eight comparators for each pixel verifying whether the total charge collected is higher than in its neighbours [11].

This specific pixel's architecture and algorithms implemented enables chip manufacturing in submicron technologies maintaining the same functionality in smaller pixel size, despite nonuniformity of analog parameters and charge sharing between pixels.

In the multichannel integrated circuits designed for X-ray detection, it is also important to measure the pulse amplitude. Therefore, in future we plan to use ADC of 4-6 bits resolution. So far, concerning the nanometer technology in which the chip is designed, the most important aspects are the ADC circuit area as well as the signal processing speed and power consumption. Taking into account these requirements new ADC solutions are currently tested [8].

Another aspect aforementioned for X-ray applications is 3D technology. The first chip for X-ray photon counting has been already designed in a 130 nm process. It was the first three dimension readout chip for pixel detectors, which may find its application in X-ray Photon Correlation Spectroscopy experiments (XPCS) on light sources [12]. The similar analog blocks architecture and the algorithms implemented makes designing the 3D chip in 40 nm technology possible in the near future.

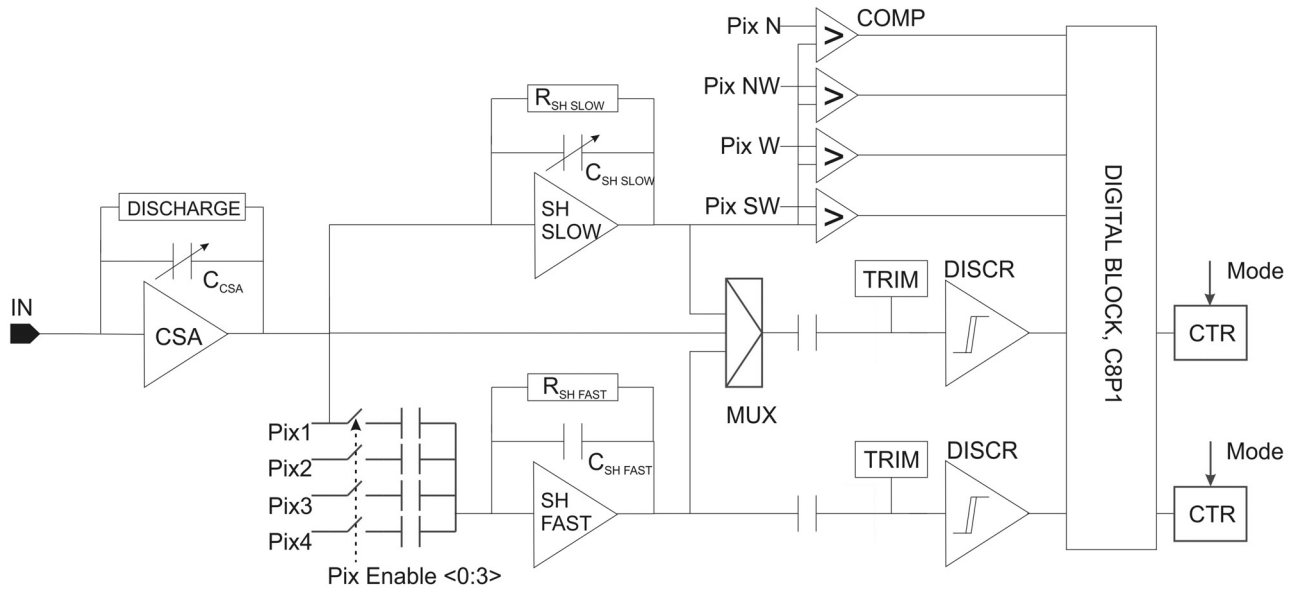

Figure 2. The readout channel architecture of the proposed chip

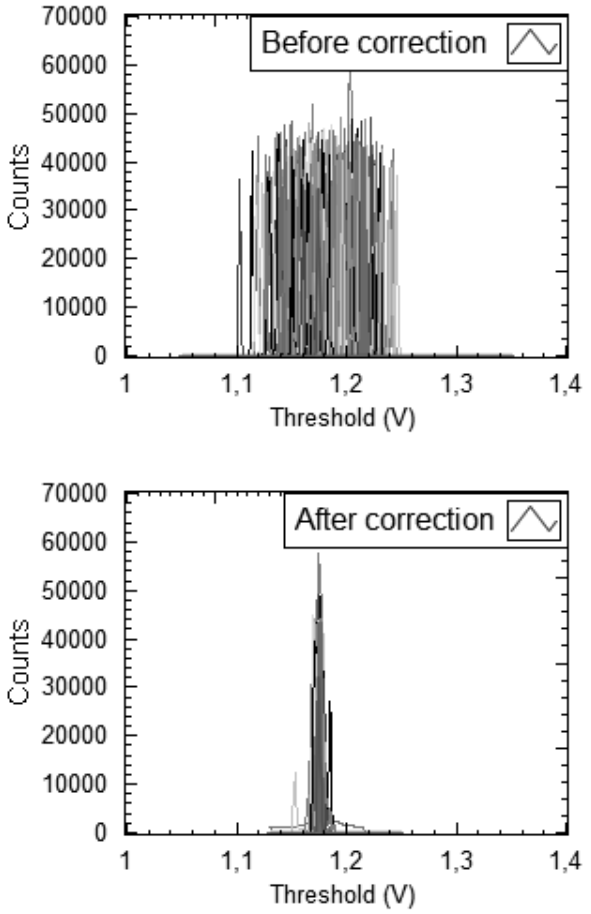

Figure 3. Results of threshold scans before and after correction

The improvement that should be also considered is using SOI technology. This solutions is more expensive but the advantages for pixel detectors are worth trying. The reduction of current leakage and signal noise is vital for medical applications, since it improves the image quality and consequently supports more accurate diagnosis. Increasing the speed of the chip is also very important considering the reduction of patient's exposure time to the radiation.

Conclusions and future study

In the article Authors presented new trends in hybrid pixel detectors for X-ray imaging and showed how proposed solution is working taking the advantage of submicron technologies and how it may be improved in the future using other new techniques, for example SOI and 3D technology. The aspects of chip implementation, including charge sharing compensation techniques are discussed in details, the experimental results for trimming DAC correction are presented and new possible solutions for readout electronics like ADC implementation are taken into consideration.

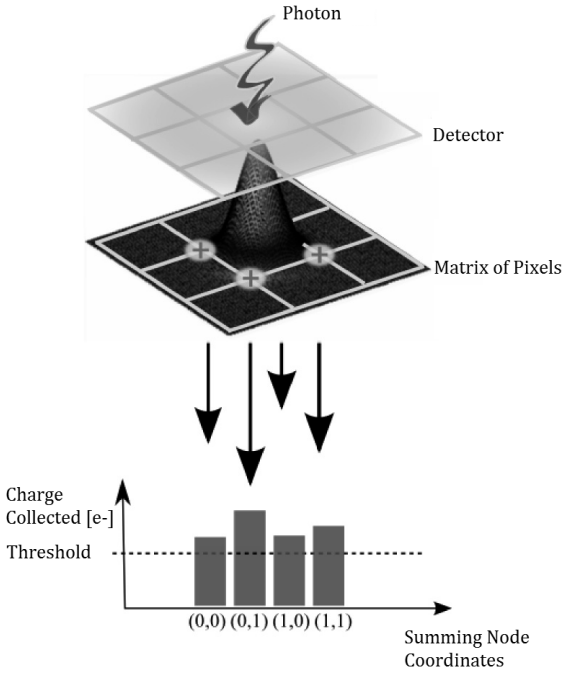

Figure 4. Pixel detector and matrix of IC pixels. After the photon hit charge cloud may be collected by up to 4 neighbour pixels. The charge from 4 pixels is summed in the summing node and then compared to the threshold

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