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IMPLEMENTATION OF BULK-DRIVEN CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (BD-CDTA)

This paper presents a new high performance Bulk-Driven current differencing transconductance amplifier (BD-CDTA), a recently reported active element, especially suitable for analog signal processing applications. The proposed BD-CDTA provides high output impedances at port Z and X, excellent input/output current tracking. The proposed BD-CDTA circuit operates at supply voltages of ± 0.6V. PSPICE simulation results using TSMC 0.18 μm CMOS process model are included to verify the expected values.

KEYWORDS: Bulk-Driven transistors, Low-voltage, Low-power CDTA, PSPICE simulation

1. INTRODUCTON

Recently, a new current-mode active building block, which is called as a current differencing transconductance amplifier (CDTA), has been proposed [1]. This device that has two current inputs and two kinds of current output provides an easy implementation of current-mode active filters [2]. It also exhibits the ability of electronic tuning by the help of its transconductance gain (gin). All these advantages together with its current-mode operation nature make the CDTA a promising choice for realizing the current-mode filters. As a result, many implementations of CDTA-based circuits have also been developed by various researchers [2-5].

In this paper, a new improved CMOS configuration of CDTA is presented providing low input impedances at ports p and n, very high out impedances at ports z and x, a good linearity and high input/output gain ratio for current transfer. The CDTA offered contains only MOS transistors and is designed to be implemented in CMOS technology. The next sections include the PSPICE simulations of the CDTA device characteristics, and the filter characteristics. The simulations show that the proposed CDTA circuit exhibits a very good performance.

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2. CDTA

The CDTA element [1] with its schematic symbol in Fig. 1 (a) has a pair of low-impedance current inputs p and n, and an auxiliary terminal z, whose outgoing current is the difference of input currents. Also in Fig. 1 (b) is given a possible implementation of CDTA using the OTA components. Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance gm and the voltage at the z terminal gives their magnitudes.

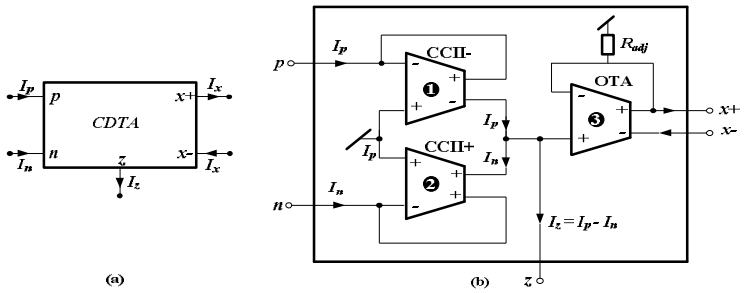

Fig. 1. (a) Symbol of the CDTA, (b) its implementation by bulk-driven OTAs

Therefore, this active element can be characterized with the following equations:

$$V_p = V_n = 0 \qquad I_z = I_p - I_n \tag{1}$$

$$I_{x+} = \boldsymbol{g}_m V_Z \qquad I_{x-} = -\boldsymbol{g}_m V_Z \tag{2}$$

where $V_z = I_z.Z_z$ and Z_z is the external impedance connected to Z terminal of the CDTA. CDTA can be thought as a combination of a current differencing unit [6] followed by a dual-output operational transconductance amplifier, DO-OTA. Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by $I_x = g_m(V_+ - V_-)$, where Ix is output current, V_+ and $V-$ denote non-inverting and inverting input voltage of the OTA, respectively.

CDTA applications do not require the use of external resistors, which are substituted by internal transconductors. Analogously to the well-known "g_mC" applications, the "CDTA-C" circuits are formed by CDTA elements and grounded capacitors. Such structures are well-suited for on-chip implementation.

Marking the voltages of p, n, x, and z terminals in Fig. 1 (a) with symbols V_p, V_n, V_x, and V_z, then for the CDTA+- element the following equations are true:

$$\begin{pmatrix} I_Z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 & -1 \\ \mathbf{g}_m & 0 & 0 & 0 & 0 \\ -\mathbf{g}_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{pmatrix} \tag{3}$$

3. CMOS REALIZATION BD-CDTA

In literature some linear transconductance elements are presented [7, 8]. A possible CMOS based CDTA circuit realisation suitable for the monolithic IC fabrication is displayed in Fig. 2.

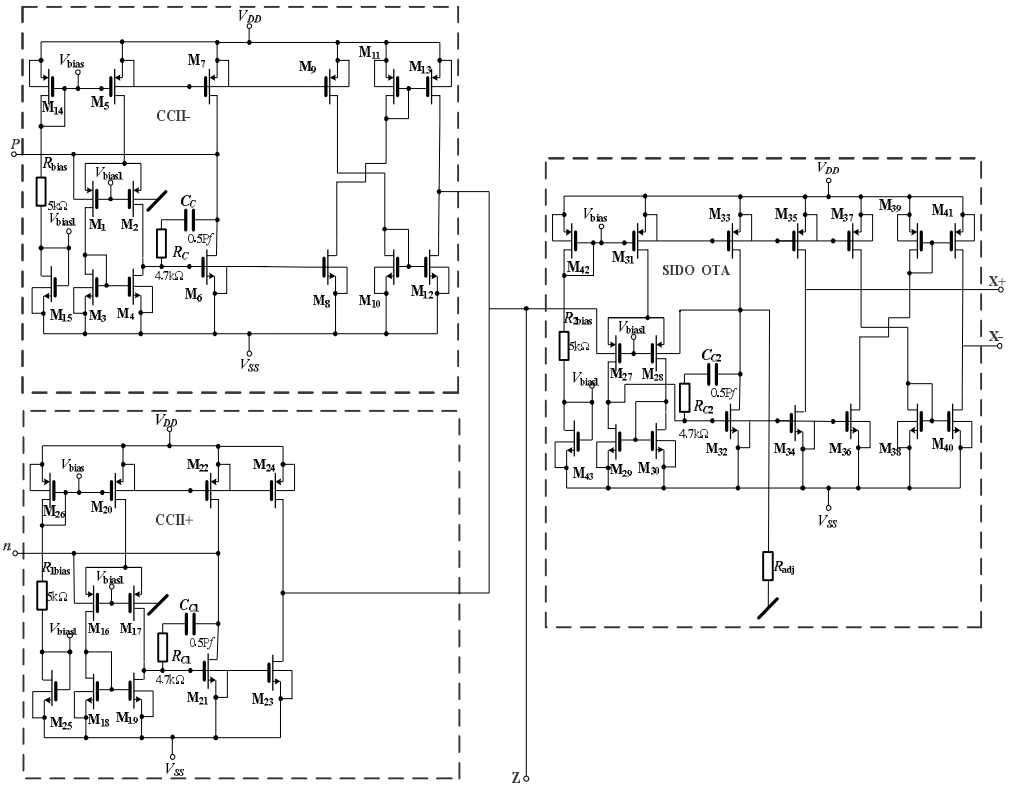

Fig. 2. The CMOS implementation of bulk-driven CDTA.
V_{DD}& V_{SS} = ±0.6V, R_{bias} = R_{1bias}= R_{2bias}= 5kΩ, R_C = R_{C1}=R_{C2} = 4.7kΩ, C_C = C_{C1}= C_{C1}=0.5Pf

A CMOS bulk-driven CDTA, designed in the 0.18 μm CMOS technology, is shown in Fig. 2. In comparison with the conventional gate-driving method, this topology works with a lower power supply voltage (±0.6 V), which also results in low power dissipation (264 μW for the complete topology in Fig. 2). Since the bulk-driving principle is applied to conventional MOS transistors, there is no need to use the expensive twin-tub technology [9]. The transistor aspect ratios are summarized in Table 1.

In Fig. 2, the DC biasing of the topology is provided by transistors M_{14}, M_{15}, M_{25}, M_{26}, M_{42}, and M_{43}, resistors R_{bias}, R_{1bias}, and R_{2bias}, and the corresponding transistors for current mirroring.

Table 1. Aspect ratios of the transistors used in the CDTA in Fig. 2

Transistor	Length (μm)	Width (μm)
M_1,M_2, M_{16},M_{17}, M_{27},M_{28}	2	30
M_3,M_4, M_{18},M_{19}, M_{29},M_{30}	2	4
M_5,M_{14}, M_{20},M_{26}, M_{31},M_{42}	3	20
M_6,M_8, M_{10},M_{12}, M_{21},M_{23}, M_{32}, M_{34}, M_{36}, M_{38}, M_{40}	2	16
M_7,M_9, M_{11},M_{13}, M_{22},M_{24}, M_{33}, M_{35}, M_{37}, M_{39}, M_{41}	3	40
M_{15},M_{25}, M_{43}	3	10

OTA No. 1 (2) in Fig. 1 (b) is implemented via transistors M_1-M_{15} and M_{16}-M_{24}. The remaining transistors (M_{27}-M_{43}) form differential-output OTA No. 3 from Fig. 1 (b) with the linearizing negative feedback led from the current output of the M_{32}-M_{33} pair to the inverting voltage input of OTA No. 3 (bulk of M_{28}). Each OTA is of the classical two stage topology, with the bulk-driven differential input stage employing a p-channel MOS transistor pair and current mirror acting as an active load, and with current inverters and circuits for providing copies of the output current.

The negative feedback from the drain of M_6 to the inverting voltage input of OTA No. 1 (bulk of M_1) is accompanied by the R_1-C_1 circuit necessary for frequency compensation [10]. The same compensation is provided for OTA No. 2 (see the R_2-C_c compensating circuit). The purpose of the compensation capacitor is to split the parasitic poles of two adjacent OTA stages in order to make the pole of the first stage dominant whereas the pole of the second stage is pushed at a high frequency.

4. SIMULATION RESULTS

The simulation results for the CDTA are given in Figs. 3 to 8. Fig.3 shows the I_z/I_p and I_z/I_n curves of the Current Differencing Unit (CDU), simulated on the assumption of $V_z = 0$. Note that for positive input currents I_p and I_n, the boundary of linear operation is ca 16 μA. The current offset ΔI_z is ca -141 nA. For the bias point $I_p = I_n = 0$, the corresponding small-signal current gains are as follows: $\alpha_p = I_z/I_p = 0.986$, $\alpha_n = I_z/I_n = 1$.

The frequency responses of current gains I_z/I_p, I_z/I_n are given in Fig. 4. The cut off frequencies for the gains α_p and αn are 22 MHz and 75 MHz, respectively. The voltage-current characteristic of the p-terminal input gate of the CDTA is shown in Fig. 5. Identical results also hold for the n-terminal. Note that when the input current approaches a value of ca 17μA, the clipping property of this curve can cause a significant nonlinear distortion. However, the range of linear operation is suitable for many applications that need extra low power consumption.

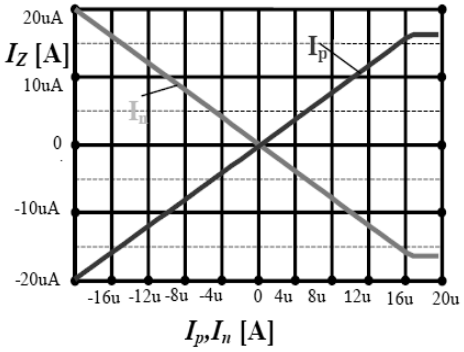

Fig. 3. DC curves I_z versus I_p or I_n, for $V_z = 0$

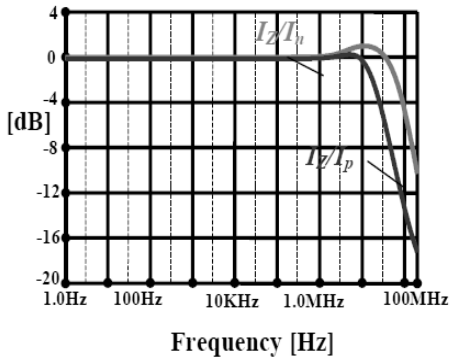

Fig. 4. Frequency responses of current gains I_z/I_p and I_z/I_n for $V_z = 0$

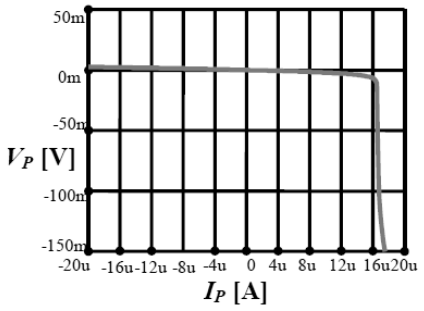

Fig. 5. DC curve V_p versus I_p for evaluating small-signal input resistance of the p- terminal

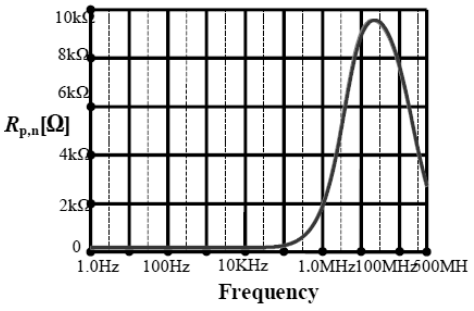

Fig. 6. Frequency dependence of the impedances of p- and n- terminals

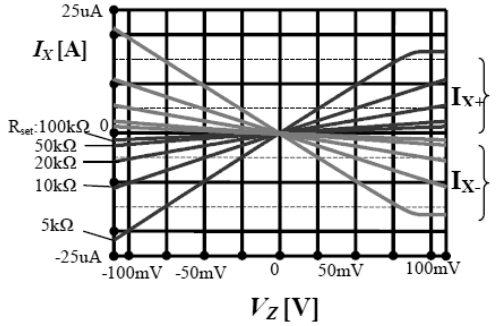

Fig. 7: DC characteristics of OTA No. 3 with R_{set} linearization and transconductance control

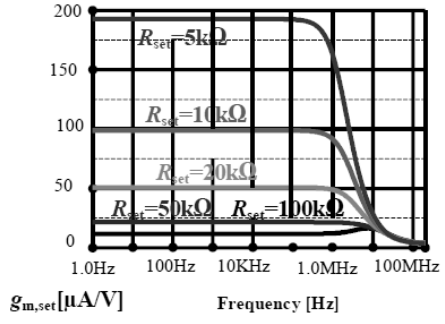

Fig. 8: Frequency responses of transconductance

For the DC bias $I_p = 0$, the small-signal resistances R_p and R_n are 166 Ω. The frequency dependences of the impedances of p- and n- terminals in Fig. 6 show that the above values are kept up to ca one hundred kilohertz. Then the

impedances increase due to the frequency dependence of the OTA transconductance.

The I_x versus V_z curves in Fig. 7 are analyzed for several values of the external resistance Rset. They clearly show the transconductance control via R_{set} as well as the effect of the linearization and increasing the dynamic range with increasing values of R_{set}. A detailed analysis also confirms that the current offset is decreasing with increasing value of Rset. For R_{set}=10 kΩ, the offset current is only -141nA. Fig. 8 show the frequency dependences of $g_{m,set}$ and of the x- and z-terminal impedances. The transconductance bandwidth increases with increasing R_{set}. For example, *Rset*=10 kΩ yields $g_{m,set} \approx 99$ μA/V and the -3dB cutoff frequency is approximately 1.1MHz. The frequency dependence of the z-terminal impedance shows the value 277 kΩ, with a -3dB cutoff frequency of about 2 MHz. The low-frequency x-terminal resistance is ca554kΩ. Simulation results of the CDTA are summarized in Table 2.

Table 2. Simulation results of the Bulk-driven CDTA

Characteristics	Simulation Result
Power consumption	264 μW
3dB bandwidth I_Z/I_p, I_Z/I_n	22 MHz, 75MHz
DC current range I_p, I_n	±16 μA
DC voltage range V_Z(R_{set} =10 kΩ)	+170 mV, -310 mV
DC offset of OTA stage (R_{set} =10 kΩ)	-141 nA
Current gains I_Z/I_p, I_Z/I_n	0.986, 1
g_m (R_{set} =10 kΩ)	98.9 μA/V
3dB bandwidth g_m(R_{set} =10 kΩ)	1.2 MHz
Node *n* and *p* parasitic DC resistance	166 Ω
Node *z* parasitic DC resistance	277 kΩ
Node *x* parasitic DC resistance	554 kΩ
Measurement condition: V_{DD} = 0.6 V, V_{SS} = 0.6 V	

5. CONCLUSIONS

The Bulk-driven Current Differencing Transconductance Amplifier (BD-CDTA) principle which is suitable for Low Voltage LV Low Power LP circuit design is presented in this paper and the unique with the Bulk-driven MOSTs is that, it could be used in ultra-LV ultra-LP design where the voltage supply could be even below 600 mV and power consumption below 264 μW.

The main advantages of the bulk-driven devices are extra low supply voltages and power consumption. These features are achieved at the cost of lower bandwidth. That is why the proposed CDTA can find applications in

devices for frequency ranges of up to hundreds of kHz, where extra-low power consumption is required.

This circuit is designed for low frequency application. SPICE simulation of the circuit confirms the theoretical conclusions.

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