Optimization of logic circuit of Moore FSM on CPLD

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Abstract

Method of decrease of number of PAL macrocells in the circuit of Moore FSM is proposed. Method is based on usage of free outputs of embedded memory blocks to represent the code of the class of the pseudoequivalent states. Proposed approach permits to decrease the hardware amount without decrease of digital system performance. An example of application of proposed method is given.

Keywords: Moore finite-state-machine, PAL macrocells, CPLD, embedded memory blocks, flow-chart of algorithm.

Optymalizacja skończonych automatów Moore’a w układach CPLD

Streszczenie

W pracy przedstawiona została metoda zmniejszania ilości makrokomórek w układach typu PAL przy pomocy Moore’a FSM. Metoda ta jest oparta na wykorzystaniu nieużywanych wyjść osadzonych obszarów pamięci w celu reprezentacji kodu klasy pseudo-równoważnych stanów. Zaproponowane podejście pozwala zmniejszyć ilość wymaganego zużycia sprzętu bez zmniejszenia wydajności systemów cyfrowych. Podany również jest przykład aplikacji zaproponowanego rozwiązania.

Słowa kluczowe: automat Moore’a, PAL makro-komórka, CPLD, wbudowany blok pamięci, schemat blokowy algorytmu.

1. Introduction

A control unit is very important block of any digital system, its function is coordination of other blocks interplay [1, 7]. A model of Moore finite-state-machine (FSM) is used very often to represent the control unit [5, 6]. The current state of microelectronics permits to implement a complex digital system using single chip of the “system-on-a-chip” (SoC) type [11, 12]. An arbitrary logic of a digital system can be implemented using PAL (programmable array logic) macrocells of SoC, if they used CPLD (complex programmable logic devices) approach [8]. The tabular functions can be implemented using embedded memory blocks of the SoC [5]. One of actual problems is decrease of the hardware amount in the logic circuit of control unit [6].

The solution of this problem permits to decrease the chip area occupied by circuit of control unit and it gives the potential possibility to increase the amount of digital system functions inside single chip. The pecularities of both PAL macrocells and model of control unit should be taking into account to solve this problem [5]. The pecularities of PAL are wide fan-in of macrocells and very limited number of terms per macrocell [10, 12]. The pecularities of Moore FSM are existence of pseudoequivalent states and regular character of system of microoperations that permits its implementation using embedded memory blocks [2, 3]. In this article we propose the method of optimization of the amount of PAL macrocells in the logic circuit of Moore FSM using the above mentioned pecularities.

2. Background of Moore FSM design

Let control algorithm of digital system is specified by flow-chart of algorithm (FCA) [6] \( \Gamma = (B, E, \gamma) \), where \( B = \{ b_0, b_1, \ldots, b_i \} \subseteq E \cup \{ E \} \) is set of the vertices and \( E \) is set of the edges. Here \( b_0 \) is initial vertex, \( b_i \) is final vertex, \( E \) is set of operational vertices, \( E \) is set of conditional vertices. The vertex \( b_i \in E \) contains a collection of microoperations \( Y(b_i) \leq Y \), where \( Y = \{ y_1, \ldots, y_k \} \) is set of microoperations of data-path [7] of digital system. The vertex \( b_i \in E \) contains a logic condition \( x_i = X \), where \( X = \{ x_1, \ldots, x_k \} \) is set of logic conditions (flags) [1]. The initial and final vertices of FCA correspond to initial state \( a_i = A \), where \( A = \{ a_0, \ldots, a_\delta \} \) is set of internal states of Moore FSM. Each operational vertex \( b_i \in E \) corresponds to unique state \( a_i \in A \) and collection \( Y(b_i) = Y(a_i) \). The logic circuit of Moore FSM \( U_1 \) set up by systems of Boolean functions:

\[
\phi = \phi(T, X),
\]

\[
Y = Y(T),
\]

where \( T = \{ T_1, \ldots, T_k \} \) is set of internal variables to encode the states \( a_i \in A \), \( R = \log_2 M \); \( \phi = \{ D_1, \ldots, D_k \} \) is set of excitation functions of the FSM memory.

The structural diagram of Moore FSM \( U_1 \) is shown in Fig. 1.

![Fig. 1. Structural diagram of Moore FSM U1](image)

Rys. 1. Struktura diagramu Moore’a FSM \( U_1 \)

Here combinational circuit CC forms functions (1), which are the excitation functions of D flip-flops of register RG. Circuit CMO forms microoperations (2). The Pulse Start is used to load the code of initial state into RG, pulse Clock is used to change the
content of RG from code \( K(a_n) \) of current state \( a_n \in A \) to code \( K(a_Q) \) of the next state \( a_Q \in A \). In case of CPLD-based SoC circuit CC is implemented using PAL macrocells and circuit CMO is implemented using embedded memory blocks [12]. The base to form the systems (1)-(2) is the direct structural table (DST) [7] with columns: \( a_n \) is current state of FSM; \( K(a_n) \) is code of current state having \( R \) bits; \( a_Q \) is state of transition, \( K(a_Q) \) is code of this state; \( \gamma \) is conjunction of some elements of the state \( s \) or (their complements), that causes transition \( \wedge a_n \wedge a_Q; \Phi \subseteq \Phi_c \) collection of excitation functions that are equal to 1 to switch RG from \( K(a_n) \) into \( K(a_Q) \); \( h \) is number of transition \( (h = 1, \ldots, H(\Gamma)) \). The column \( a_n \) contains the collection \( \gamma(a_n) \subseteq \gamma \).

As a rule, the number of transitions \( H(\Gamma) \) exceeds the number of transitions \( H(\Gamma) \) of equivalent Mealy FSM [2]. It leads to increase of the amount of PAL macrocells (hardware amount) and sometimes number of levels in the circuit CC of Moore FSM in comparison with these characteristics of equivalent Mealy FSM [5]. The value \( H(\Gamma) \) can be decreased by taking into account the existence of pseudo-equivalent states of Moore FSM [1]. The states \( a_{\alpha_1} \in A \) are pseudo-equivalent states, if the outputs of corresponding operational vertices are connected with the input of the same vertex of FCA \( \Lambda \). Let \( \Pi = \{B_1, \ldots, B_l\} \) is partition of the set \( A \) by classes of pseudo-equivalent states \( (\ell \leq M) \). Let us encode the class \( B_i \in \Pi \) by binary code \( K(B_i) \) with \( R_1 = \log_2(I) \) bits. Let us use the variables \( \tau \in \tau \) for such encoding, where \( |\tau|=R_1 \).

In this case special code transformer TC can be introduced into circuit of \( U_1 \). It forms the codes \( K(B_i) \) on the base of the codes \( K(a_n) \), where \( a_n \in B_i \). Now circuit CC forms functions

\[
\Phi = \Phi(\tau, X),
\]

and circuit TC forms functions

\[
\tau = \tau(T).
\]

The circuit TC is implemented using embedded memory blocks of SoC [5].

It is proved, that system (3) has \( H(\Gamma) \) terms [2]. But such approach has one drawback: it consumes additional resource of embedded memory blocks to implement the circuit of TC.

In this work we propose the design method that permits to decrease the hardware amount in the circuit CC without code transformer. The proposed method is based on the following peculiarities of CPDL [8, 10, 12]:
- the fan-in of PAL macrocells exceed significantly the maximal possible number of literals in the terms of the system (1), that is equal to \( \log_2(R) \);
- the number of outputs of embedded memory block can be chosen from some restricted area \( \{1, 2, 4, 8\} \).

3. Main idea of proposed method

Let \( t_f \) is fixed number of outputs of the embedded memory block and let \( q \) is amount of its words, if \( t_f = 1 \). The value \( t_f \) for FSM \( U_1 \) is determined as

\[
t_f = \lceil q/M \rceil.
\]

The total amount of the outputs \( t_s \) of all embedded memory blocks in the circuit is determined as

\[
t_s = \lceil N/t_f \rceil \ast t_f.
\]

In this case

\[
\Delta = t_s - N
\]

outputs are not in use to represent the microoperations \( \gamma \in \gamma \).

Let us represent the set \( \Pi_4 = \Pi_B \cup \Pi_C \), where \( B_i \in \Pi_B \), if condition

\[
|B_i| > 1
\]

holds, and \( B_i \in \Pi_C \), if condition (8) is violated. It is clear that block TC should forms only the codes of the classes \( B_i \in \Pi_B \). Let us encode each class \( B_i \in \Pi_B \) by binary code \( K(B_i) \) with

\[
R_2 = \log_2(M_t + 1)
\]

bits, where \( |M_t| = \Pi_B \) and “1” is added to indicate the case, when \( B_i \in \Pi_B \). Let us use the variables \( z \in Z \) for such encoding, where \( |Z| = R_2 \). Let us discuss the case, when condition

\[
\Delta \geq R_2
\]

holds. In this case FCA \( \Gamma \) can be interpreted by proposed Moore FSM \( U_2 \) (Fig. 2).

![Fig. 2. Structural diagram of Moore FSM U2](image)

Rys. 2. Struktura diagramu Moore’a FSM \( U_2 \)

Here circuit CC forms functions

\[
\Phi = \Phi(T, Z, X),
\]

and circuit CMO forms functions (2) and functions

\[
Z = Z(T).
\]

The variables \( T_e \in T \) represent the codes \( K(a_n) \), where \( a_n \in B_i \). Such approach permits to decrease the number of terms in the system \( \Phi \) up to \( H(\Gamma) \) and number of embedded memory blocks are equal for both CMO and CMOCC. As we can see, circuit \( U_2 \) does not include the TC. The number of inputs in the PAL macrocells of \( U_2 \) is increased up to \( L + R + R_2 \), but it does not affect the hardware amount in the circuit CC in comparison with Moore FSM with TC. The cycle time of both \( U_1 \) and \( U_2 \) is the same in the worst case. In the best case, if circuit CC of \( U_2 \) has less levels, than circuit CC of \( U_1 \), the time of cycle of \( U_2 \) is less, that time of cycle of \( U_1 \). Therefore, the proposed approach permits to decrease hardware amount without decrease of digital system performance.

The method of design of logic circuit of \( U_2 \) differs from design method of \( U_1 \) [6] only in some details. They are connected with estimations of values (7), (9), (10) and construction of modified DST (MDST) to form the functions (11). Let us discuss an example of design of Moore FSM \( U_2(\Gamma) \), where symbol \( U(\Gamma) \) stays for interpretation of FCA \( \Gamma \), by Moore FSM with structure \( U_1 \).

4. Example of proposed method application

Let control algorithm of a digital system is represented by marked FCA \( \Gamma_1 \), where \( M = 16 \). Let FCA \( \Gamma_1 \) is set up by system of formulae of transitions [6], where vertices \( b_i \in E_2 \) are replaced by corresponding states \( a_n \in A \):

\[
a_1 \rightarrow a_2; a_2 \rightarrow a_3; a_3 \rightarrow a_4; a_4 \rightarrow a_5; a_5 \rightarrow a_1;
a_6 \rightarrow x_1x_2x_3; V x_1x_2; V x_3x_4; V x_5x_6; V x_7x_8x_9;
a_7 \rightarrow x_1x_2x_3; V x_1x_2x_3; V x_4x_5x_6x_7x_8x_9;
a_8 \rightarrow x_1x_2x_3; V x_1x_2x_3; V x_4x_5x_6x_7x_8x_9;
a_9 \rightarrow x_1x_2x_3; V x_1x_2x_3; V x_4x_5x_6x_7x_8x_9;
a_{10} \rightarrow x_1x_2x_3; V x_1x_2x_3; V x_4x_5x_6x_7x_8x_9;
\]

(13)

It is follows from (13) that \( M = 16, R = 7, |\Phi| = 4, \Pi = \{B_1, \ldots, B_8\} \), where \( B_1 = \{a_1\}, B_2 = \{a_2\}, B_3 = \{a_3\}, B_4 = \{a_4, a_5, a_6\}, B_5 = \{a_7\}, B_6 = \{a_8, a_9, a_{10}\}, B_7 = \{a_{11}, a_{12}, a_{13}, a_{14}\}, B_8 = \{a_{15}\} \).

Let \( N = \{t_f \} = 4 \), then \( q = 64 \). An analysis of \( \Pi_4 \) gives us \( \Pi_B = \{B_6, B_8, B_7\} \) and \( \Pi_C = \{B_1, B_2, B_3, B_5, B_8\} \).
Therefore, $M = 3$, $R_2 = |z| = 2$ as it follows from (9). The condition (10) holds and application of proposed method has sense.

Let microoperations $y_4 \in Y$ are distributed among the states of FSM in the following order: $Y(a_1) = \emptyset$, $Y(a_2) = Y(a_3) = \{y_1, y_2\}$, $Y(a_4) = \{y_4, y_5\}$, $Y(a_5) = Y(a_6) = \{y_3, y_7\}$, $Y(a_7) = \{y_7, y_8\}$. Let us encode the classes $B_i \in \Pi_k$ in the following manner: $K(B_1) = 0$, $K(B_2) = 10$, $K(B_3) = 11$. The code $<00>$ corresponds to all blocks $B_i \in \Pi_0$. Let states of FSM are encoded in a trivial way: $K(a_1) = 0000$, ..., $K(a_6) = 1111$. Let code $K(B_i)$, where $B_i \in \Pi_k$, is equal to code $K(a_i)$, where $a_i \in B_i$.

To form the MDST of Moore FSM $U_2$ the states $a_i \in B_i$ should be replaced by classes $B_i \in \Pi_k$ in the left parts of all formulae of transitions. Such transformation of the system (13) leads to system (14):

$$B_1 \rightarrow a_2; \, B_2 \rightarrow a_5; \, B_3 \rightarrow x_1x_2a_4 \land x_1/x_2a_5 \lor x_1/x_2a_6; \, B_4 \rightarrow a_6; \, B_5 \rightarrow x_5/x_6a_7 \land x_5/x_6a_8 \lor x_5/x_6a_9; \, B_6 \rightarrow a_9; \, B_7 \rightarrow a_{10},$$

The MDST includes the columns: $B_i, K(B_i), K(a_i), a_i, K(x_i), x_i, \phi_i, h$.

In case of Moore FSM $U_2(\Gamma)$ this table has $U_2(\Gamma) = 18$ lines. The first 6 lines of MDST are shown in Table 1.

<table>
<thead>
<tr>
<th>$B_i$</th>
<th>$K(B_i)$</th>
<th>$K(a_i)$</th>
<th>$x_i$</th>
<th>$\phi_i$</th>
<th>$h$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B_1$</td>
<td>0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$B_2$</td>
<td>0001</td>
<td>0001</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$B_3$</td>
<td>0100</td>
<td>0111</td>
<td>x_1/x_2</td>
<td>D_3</td>
<td></td>
</tr>
<tr>
<td>$B_4$</td>
<td>0101</td>
<td>0101</td>
<td>x_1/x_2</td>
<td>D_5</td>
<td></td>
</tr>
<tr>
<td>$B_5$</td>
<td>0110</td>
<td>0110</td>
<td>x_1/x_2</td>
<td>D_6</td>
<td></td>
</tr>
</tbody>
</table>

This table is the base to form the system (11). For example, from Table 1 we can get the part of disjunctive normal form of excitation function $D_3(h)$, where

$$D_3 = z_1/z_2/T_1/T_2/T_3 \lor z_1z_2x_1x_2 \lor z_1z_2/x_1/x_2.$$

The PAL implementation of the function $D_3$ is shown in Fig. 3.

The table of CMOC includes the columns $a_i, K(a_i), Y(a_i), K(B_i), m$. It is formed in a trivial way and in case of FSM $U_2(\Gamma)$ it has $M = 16$ lines. The first 8 lines are shown in the Table 2.

<table>
<thead>
<tr>
<th>$a_i$</th>
<th>$K(a_i)$</th>
<th>$Y(a_i)$</th>
<th>$K(B_i)$</th>
<th>$m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_1$</td>
<td>0000</td>
<td></td>
<td>00</td>
<td>1</td>
</tr>
<tr>
<td>$a_2$</td>
<td>0001</td>
<td>Y(x_1)</td>
<td>00</td>
<td>2</td>
</tr>
<tr>
<td>$a_3$</td>
<td>0100</td>
<td>y_5/y_6</td>
<td>00</td>
<td>3</td>
</tr>
<tr>
<td>$a_4$</td>
<td>0111</td>
<td>y_5/y_6</td>
<td>01</td>
<td>4</td>
</tr>
<tr>
<td>$a_5$</td>
<td>0111</td>
<td>y_5/y_6</td>
<td>01</td>
<td>5</td>
</tr>
<tr>
<td>$a_6$</td>
<td>0111</td>
<td>y_5/y_6</td>
<td>00</td>
<td>7</td>
</tr>
<tr>
<td>$a_7$</td>
<td>0111</td>
<td>y_5/y_6</td>
<td>10</td>
<td>8</td>
</tr>
</tbody>
</table>

In case of $U_2(\Gamma)$ this table has $N + R_2 = 16$ outputs, each output corresponds to single bit of the output word of embedded memory block. The code $K(a_i)$ is treated as an address of embedded memory block word with one-hot codes of microoperations [3] and maximal codes of the classes $B_i \in \Pi_k$. To implement the systems (2) and (12) it is enough

$$\eta_\phi = \frac{N}{\ell_1} \cdot \lambda _k$$

blocks embedded memory circuit with $q \geq M$. In case of $U_2(\Gamma)$ we have $\eta_\phi = 3$.

The implementation of logic circuit of Moore FSM $U_2$ is reduced to implementation of system (11) using PAL macros and implementation of systems (2) and (12) using embedded memory blocks. There are effective methods of these tasks’ solution [10,12], but they are out the scope of our article.

5. Conclusion

Experiments were performed using probability based method, which is presented in [4]. Because the actual experiment is quite complicated, it is beyond the scope of this article. The proposed method permits to decrease the amount of PAL macros in the circuit that forms excitation functions of FSM memory. The researches of the authors show that this decrease is proportional to coefficient

$$\eta = H_2(\Gamma) / H_2(\Gamma).$$

Let us point out that value $H_2(\Gamma)$ is equal to the number of transitions of equivalent Mealy FSM. The application of proposed method is possible only, if condition (10) holds. Our researches shown that in this case the hardware amount in the circuit of FSM $U_2(\Gamma)$ can be up to 26-28% less, than in circuit of FSM $U_1(\Gamma)$. The main direction of the future research is comparison the proposed methods with known methods from [9, 10, 12, 13].

6. References


Artykuł recenzowany